DATA SHEET

TZA3012AHW

30 Mbits/s up to 3.2 Gbits/s A-rate™ fibre optic receiver

Preliminary specification

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Philips Semiconductors

PHILIPS

30 Mbits/s up to 3.2 Gbits/s A-rate™ fibre optic receiver

TZA3012AHW

FEATURES

- Single 3.3 V power supply
- I²C-bus and pin programmable fibre optic receiver.

Dual limiter features

- Dual limiting input with 12 mV sensitivity
- Received Signal Strength Indicator (RSSI)
- Loss Of Signal (LOS) indicator with threshold adjust
- Differential overvoltage protection.

Data and clock recovery features

- Supports SHD/SONET rates at 155.52, 622.08, 2488.32 and 2666.06 Mbits/s (STM16/OC48 + FEC)
- Supports Gigabit Ethernet at 1250 and 3125 Mbits/s
- Supports Fibre Channel at 1062.5 and 2125 Mbits/s
- ITU-T compliant jitter tolerance
- Frequency lock indicator
- Stable clock signal at the absence of input data
- Recovered data and clock loop mode outputs.

Demultiplexer features

- 1 : 16, 1 : 10, 1 : 8 or 1 : 4 demultiplexing ratio
- LVPECL or CML demultiplexer outputs
- Frame detection for SDH/SONET and GE frames
- Parity bit generation
- Loop mode inputs on demultiplexer.

Additional features with the I2C-bus

- A-rate™(1): supports any bit rate from 30 Mbits/s to 3.2 Gbits/s with one single reference frequency
- Programmable with frequency resolution of 10 Hz
- 4 reference frequency ranges
- Adjustable swing of data, clock and parallel outputs
- Programmable polarity of all RF I/Os
- Swap of all RF I/O's for optimal connectivity
- Swap of parallel bus for optimal connectivity
- Slice level adjustment to improve Bit Error Rate (BER)
- Mute function for a forced logic 0 output state
- Programmable parity
- Programmable 32 bits frame detection.

APPLICATIONS

- Any optical transmission system with bit rates between 30 Mbits/s and 3.2 Gbits/s
- Physical interface IC in receive channels
- Transponder applications
- Dense Wavelength Division Multiplexing (DWDM) systems.

(1) A-rate is a trademark of Philips Semiconductors

GENERAL DESCRIPTION

The TZA3012AHW is a fully integrated optical network receiver, containing a dual limiter, Data and Clock Recovery (DCR) and a demultiplexer with the ratios 1 : 16, 1 : 10, 1 : 8 or 1 : 4.

The A-rate feature allows the IC to operate at any bit rate between 30 Mbits/s and 3.2 Gbits/s with one single reference frequency. The receiver supports loop modes with serial clock and data inputs and outputs. All clock signals are generated using a fractional N synthesizer with 10 Hz resolution giving a true, continuous rate operation. For full configuration flexibility, the receiver can be programmed via the I²C-bus.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TZA3012AHW	HTQFP100	plastic, heatsink thin quad flat package; 100 leads; body 14 × 14 × 1.0 mm	SOT638–1

BLOCK DIAGRAM

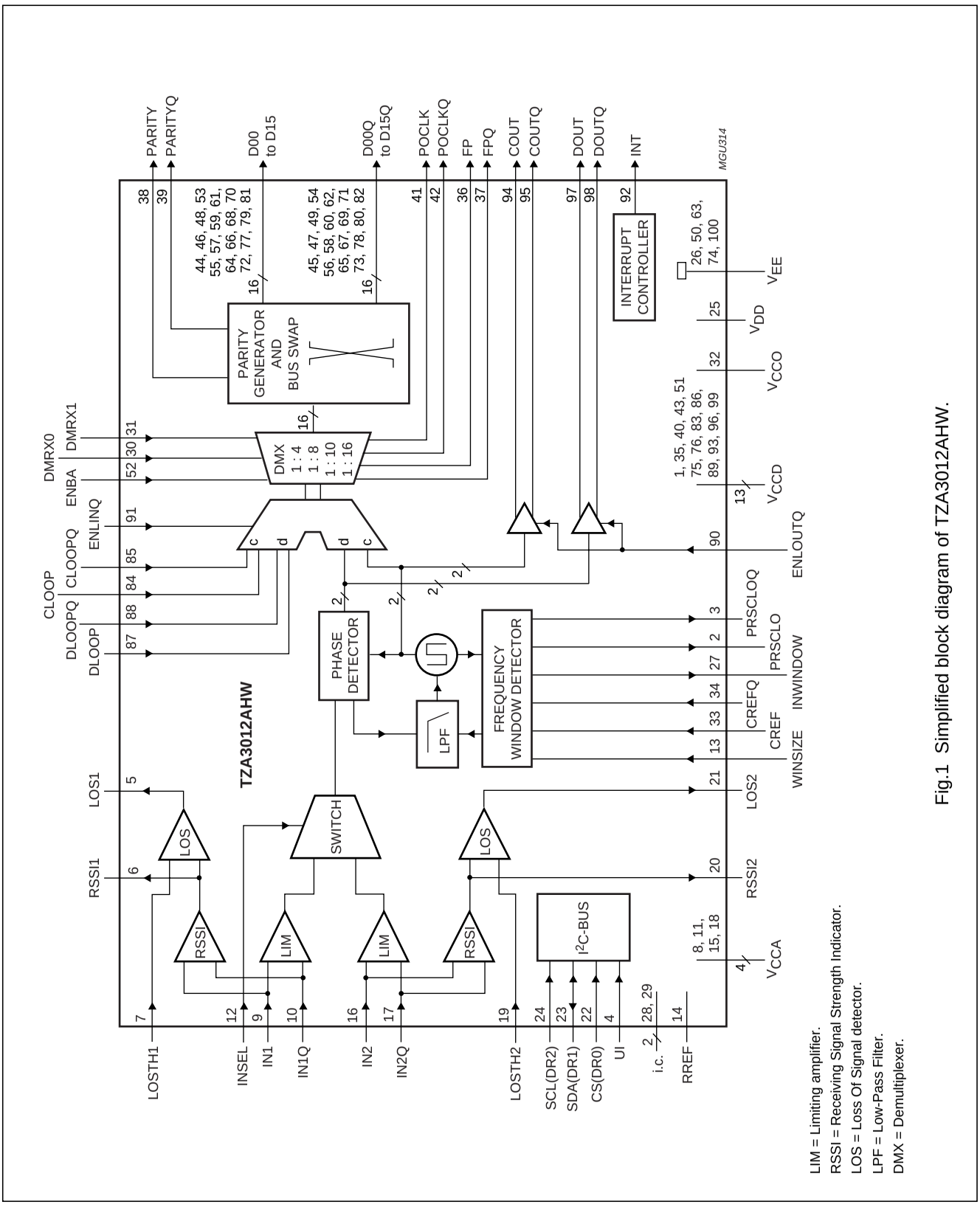


Fig.1 Simplified block diagram of TZA3012AHW.

LIM = Limiting amplifier.
RSSI = Receiving Signal Strength Indicator.
LOS = Loss Of Signal detector.
LPF = Low-Pass Filter.
DMX = Demultiplexer.

PINNING

SYMBOL	PIN	DESCRIPTION
V_{EE}	die pad	common ground plane
V_{CCD}	1	supply voltage (digital part)
PRSCLO	2	prescaler output
PRSCLOQ	3	prescaler output inverted
UI	4	user interface selection input
LOS1	5	LOS output of first input channel
RSSI1	6	received signal strength indicator output of first input channel
LOSTH1	7	LOS threshold input for first input channel
V_{CCA}	8	supply voltage (analog part)
IN1	9	input of first channel
IN1Q	10	input of first channel inverted
V_{CCA}	11	supply voltage (analog part)
INSEL	12	input selector
WINSIZE	13	wide and narrow frequency detect window selection input
RREF	14	reference resistor input
V_{CCA}	15	supply voltage (analog part)
IN2	16	input of second channel
IN2Q	17	input of second channel inverted
V_{CCA}	18	supply voltage (analog part)
LOSTH2	19	LOS threshold input for second input channel
RSSI2	20	received signal strength indicator output of second input channel
LOS2	21	LOS output of second input channel
CS(DR0)	22	chip select (data rate select 0)
SDA(DR1)	23	I^2C-bus serial data (data rate select 1)
SCL(DR2)	24	I^2C-bus serial clock (data rate select 2)
V_{DD}	25	supply voltage (digital)
V_{EE}	26	ground
INWINDOW	27	frequency window detector output
i.c.	28	internally connected
i.c.	29	internally connected
DMXR0	30	DEMUX ratio select 0
DMXR1	31	DEMUX ratio select 1
V_{CCO}	32	supply voltage (clock generator)
CREF	33	reference clock input
CREFQ	34	reference clock input inverted
V_{CCD}	35	supply voltage (digital part)
FP	36	frame pulse output
FPQ	37	frame pulse output inverted
PARITY	38	parity output
PARITYQ	39	parity output inverted
V_{CCD}	40	supply voltage (digital part)
POCLK	41	parallel clock output
POCLKQ	42	parallel clock output inverted
V_{CCD}	43	supply voltage (digital part)
D00	44	parallel data output 00
D00Q	45	parallel data output 00 inverted
D01	46	parallel data output 01
D01Q	47	parallel data output 01 inverted
D02	48	parallel data output 02
D02Q	49	parallel data output 02 inverted
V_{EE}	50	ground

SYMBOL	PIN	DESCRIPTION
V_{CCD}	51	supply voltage (digital part)
ENBA	52	byte alignment enable input
D03	53	parallel data output 03
D03Q	54	parallel data output 03 inverted
D04	55	parallel data output 04
D04Q	56	parallel data output 04 inverted
D05	57	parallel data output 05
D05Q	58	parallel data output 05 inverted
D06	59	parallel data output 06
D06Q	60	parallel data output 06 inverted
D07	61	parallel data output 07
D07Q	62	parallel data output 07 inverted
V_{EE}	63	ground
D08	64	parallel data output 08
D08Q	65	parallel data output 08 inverted
D09	66	parallel data output 09
D09Q	67	parallel data output 09 inverted
D10	68	parallel data output 10
D10Q	69	parallel data output 10 inverted
D11	70	parallel data output 11
D11Q	71	parallel data output 11 inverted
D12	72	parallel data output 12
D12Q	73	parallel data output 12 inverted
V_{EE}	74	ground
V_{CCD}	75	supply voltage (digital part)
V_{CCD}	76	supply voltage (digital part)

SYMBOL	PIN	DESCRIPTION
D13	77	parallel data output 13
D13Q	78	parallel data output 13 inverted
D14	79	parallel data output 14
D14Q	80	parallel data output 14 inverted
D15	81	parallel data output 15
D15Q	82	parallel data output 15 inverted
V_{CCD}	83	supply voltage (digital part)
CLOOP	84	loop mode clock input
CLOOPQ	85	loop mode clock input inverted
V_{CCD}	86	supply voltage (digital part)
DLOOP	87	loop mode data input
DLOOPQ	88	loop mode data input inverted
V_{CCD}	89	supply voltage (digital part)
ENLOUTQ	90	line loop back enable input (active LOW)
ENLINQ	91	diagnostic loop back enable input (active LOW)
INT	92	interrupt output
V_{CCD}	93	supply voltage (digital part)
COUT	94	recovered clock output
COUTQ	95	recovered clock output inverted
V_{CCD}	96	supply voltage (digital part)
DOUT	97	recovered data output
DOUTQ	98	recovered data output inverted
V_{CCD}	99	supply voltage (digital part)
V_{EE}	100	ground

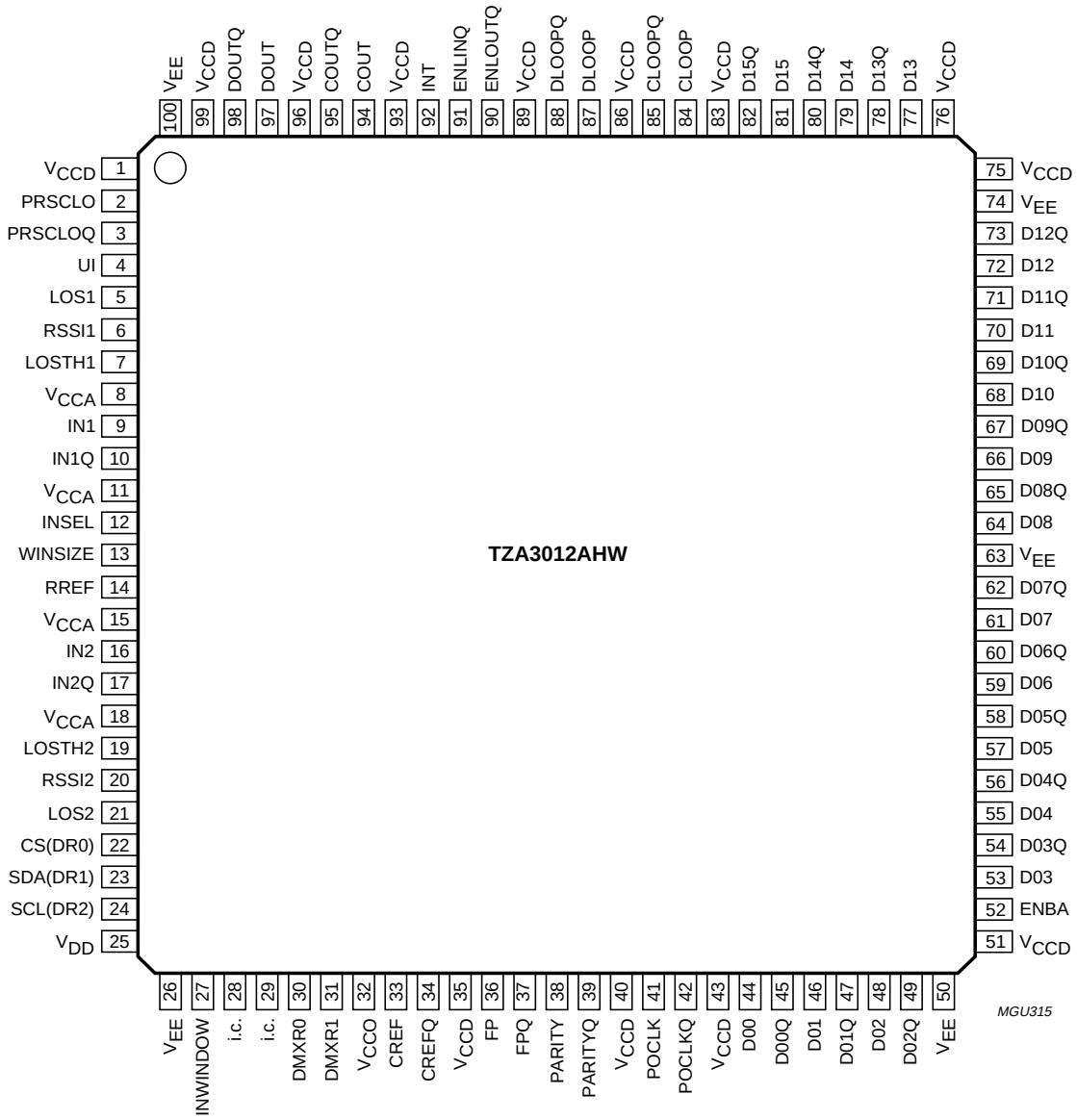


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The TZA3012AHW receives data from an incoming bit stream with a bit rate from 30 Mbits/s up to 3.2 Gbits/s. The IC has two limiting amplifier inputs. A DCR section synchronizes the internal clock generator with the incoming data. The recovered serial data and clock are demultiplexed with a ratio of 1 : 16, 1 : 10, 1 : 8 or 1 : 4.

Configuring the TZA3012AHW by I²C-bus or by pins

The IC features two types of user interface, I²C-bus control or pin programming. Interface selection is set by pin UI (User Interface); see Table 1. The I²C-bus control is operational and A-rate functionality is enabled if pin UI is left open or connected to V_{CC}. If pin UI is connected to V_{EE} pins DR0, DR1 and DR2 are available for selection of eight pre-programmed bit rates.

Table 1 Truth table for pin UI

UI	MODE	PIN 22	PIN 23	PIN 24
LOW	pre-programmed	DR0	DR1	DR2
HIGH	I²C-bus control	CS	SDA	SCL

In I²C-bus control mode, the chip is configured by using the I²C-bus pins SDA and SCL. Pin CS (chip select) has to be HIGH during I²C-bus read or write actions. When pin CS is set LOW, the programmed configuration remains active, but signals SDA and SCL are ignored. In this way, all ICs in the application with the same I²C-bus address (e.g. other TZA3012) are individually accessible. The I²C-bus address is given in Table 2.

Table 2 I2C-bus address of TZA3012AHW

A6	A5	A4	A3	A2	A1	A0	R/$\overline{W}$
1	0	1	0	0	0	0	X

A detailed list of all I²C-bus registers and the meaning of their contents can be found in Chapter “I²C-bus registers”. Some functions of the TZA3012AHW can be controlled by using a pin or the I²C-bus. In these cases, an extra I²C-bus bit called I2C<pinname> is available to set the control to the pin or to the I²C-bus bit (default is pin programmable).

If no I²C-bus control is present in the application, the IC is applicable in the ‘pre-programmed mode’, but with reduced functionality. The redefined pins DR0, DR1 and DR2 act as standard CMOS inputs that select any of the pre-programmed bit rates from Table 3 with an applied reference frequency of 19.44 MHz.

Table 3 Truth table for pins DR2, DR1 and DR0 (UI = V_{EE})

DR2	DR1	DR0	PROTOCOL	BIT RATE (Mbits/s)
LOW	LOW	LOW	STM1/OC3	155.52
LOW	LOW	HIGH	STM4/OC12	622.08
LOW	HIGH	LOW	STM16/OC48	2488.32
LOW	HIGH	HIGH	STM16 + FEC	2666.06
HIGH	LOW	LOW	GE	1250.00
HIGH	LOW	HIGH	10GE	3125.00
HIGH	HIGH	LOW	Fibre Channel	1062.50
HIGH	HIGH	HIGH	Fibre Channel	2125.00

After power-up, the TZA3012AHW initiates a Power-On Reset (POR) sequence to restore the default settings of the I²C-bus registers, regardless of the user interface. For the defaults see Table 11.

Limiting amplifiers

The TZA3012AHW contains two limiting amplifiers. The dual limiter input provides rapid switching between two line connections, supporting protection switching, for example. The active RF input is selected with pin INSEL, see Table 4. Only one channel is on at a time, the unused channel automatically goes into sleep mode, to reduce power dissipation.

Table 4 Truth table for pin INSEL

INSEL	LIMITER	SELECTED INPUT PINS
HIGH	channel 1 active	IN1(Q)
LOW	channel 2 active	IN2(Q)

Apart from pin INSEL, the input can also be selected through I²C-bus register LIMCNF (C2H), bits I2CINSEL and INSEL. Bit I2CINSEL sets pin or I²C-bus precedence and bit INSEL the actual channel selection. Again, only one channel is activated at a time. Both limiting amplifiers can be activated simultaneously by setting I²C-bus bit BOTHON of the same I²C-bus register. Although both amplifier channels are active now, only the channel selected by INSEL is used as input for the DCR section. This configuration allows very fast switching (so called ‘hot‘ switching) between the two channels. Without BOTHON switching needs 4 μs.

Table 5 Channel selection

I2CINSEL	INSEL	INSEL	SELECTED CHANNEL
I²C	PIN	I²C	
0	0	x	channel 2
0	1	x	channel 1
1	x	0	channel 2
1	x	1	channel 1

To achieve optimum receiver sensitivity for any bit rate, the bandwidth of the amplifiers is automatically scaled with the bit rate. Wideband noise of the optical front-end (photo detector and transimpedance amplifier) is thus reduced for lower bit rates. When using the I²C-bus, the bandwidth of the amplifier can be set independently of the bit rate with I²C-bus bits AMPOCT in I²C-register LIMCNF (C2H). The highest bandwidth is selected per default at power-up.

Received Signal Strength Indicator (RSSI)

The signal strength at each of the two inputs is measured with a logarithmic detector and presented at pins RSSI1 and RSSI2 for channels 1 and 2, respectively. The RSSI reading has a sensitivity of typical 17 mV/dB for a $V_{i(p-p)}$ range of 5 mV to 500 mV (see Fig.3). V_{RSSI} can be calculated using the following formula:

$$V_{RSSI} = V_{RSSI(30\ mV)} + S_{RSSI} \times 20\log\frac{V_{i(p-p)}}{30\ mV}$$

Both logarithmic detectors are active simultaneously, as opposed to the limiting amplifiers, where only one channel is active at a time. This allows the selection of the input with the strongest signal.

Loss Of Signal (LOS) indicator

Besides the analog RSSI output, a digital LOS indication is present on the TZA3012AHW. The RSSI level is internally compared with a LOS threshold, which can be set by an external resistor (pins LOSTH1 and LOSTH2) or by means of an internal D/A converter.

Bits I2CREFLVL1 and I2CREFLVL2 from I²C-bus registers BDH and BFH enable the 8-bit D/A converters, of which the value needs to be programmed into I²C-bus registers BCH (LOSTH1) or BEH (LOSTH2).

Threshold levels can be set individually for each channel. If the received signal strength is **below** the threshold value, LOS will be HIGH. A default hysteresis of 2.5 dB is applied in the comparator.

I²C-bus registers LIMLOS1CNF (BDH) and LIMLOS2CNF (BFH) provide more flexibility, i.e. a programmable hysteresis of 0 to 6 dB in steps of 0.85 dB. If needed, the polarity of the LOS outputs can be inverted by I²C-bus bits LOS1POL and LOS2POL from I²C-bus registers BDH and BFH.

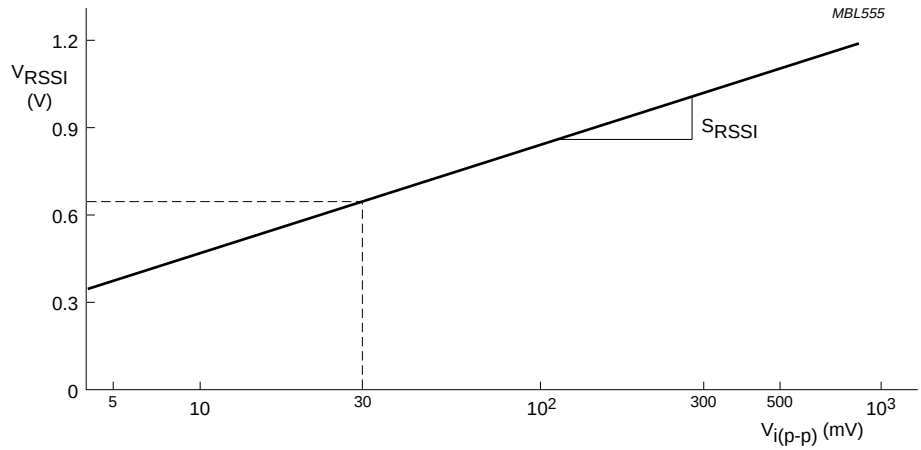


Fig.3 V_{RSSI} as a function of $V_{i(p-p)}$.

Setting LOSTH reference level by external resistor

If the built-in D/A converter is not used, the reference voltage level to pin LOSTH1 (or LOSTH2) can be set by connecting an external resistor (R2) from the relevant pin to ground. The voltage on the pin is determined by the resistor ratio between R2 and R1 (see Fig.4). For resistor R1 a value of 10 to 20 kΩ is recommended, yielding a current of 120 to 60 μA.

The LOSTH voltage equals $\frac{R2}{R1} \times V_{ref}$

Voltage V_{ref} represents a temperature stabilized and accurate reference voltage of 1.2 V. The minimum threshold level corresponds to 0 V and the maximum to 1.2 V. Hence, the value of R2 may not be higher than R1. The accuracy of the LOSTH voltage depends mainly on the matching of the two external resistors.

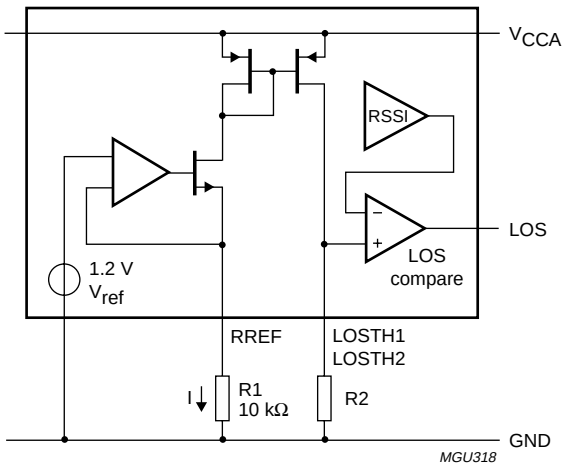


Fig.4 Setting the LOSTH reference level by external resistors.

Apart from using resistors (R1 and R2) to set the LOS threshold, an accurate external voltage source can also be used.

If no resistor is connected to LOSTH1 (or LOSTH2), or an external voltage higher than $\frac{2}{3} \times V_{CC}$ is applied to the pin, the LOS detection circuit (including the RSSI reading for that channel) is automatically switched off to reduce power dissipation. This 'auto power off' only works if UI = V_{EE}, i.e. manual control of the TZA3012AHW. In I²C-bus mode, several I²C-bus bits allow flexible configuration.

Slice level adjustment

Due to asymmetrical noise in some optical transmission systems, a pre-detection signal-to-noise ratio improvement can be achieved by adding a DC offset to the input signal. This is done by the slice level circuit in the TZA3012AHW. The required offset depends on the photo detector characteristics in the optical front-end and the amplitude of the received signal. Hence, the slice level has been made adjustable between −50 mV and +50 mV in 512 steps of 0.2 mV.

Bits SL1 and SL2 of I²C-bus registers BDH or BFH enable the slice function of the respective channel. The slice level itself is set by sign and magnitude convention. The sign, either positive or negative (polarity), is set in I²C-bus registers BDH or BFH, bits SL1SGN or SL2SGN. The magnitude, 0 to 50 mV in 256 steps, is set by an 8-bit D/A converter through I²C-bus register C0H or C1H, respectively.

The introduced offset is not present on inputs IN and INQ, in order not to affect the logarithmic RSSI detector, which would detect the offset as a valid input signal.

Data and Clock Recovery (DCR)

The TZA3012AHW recovers the clock and data contents from the incoming bit stream, see Fig.5. The DCR uses a combined frequency and phase locking scheme, providing reliable and quick data acquisition on any bit rate between 30 Mbits/s and 3.2 Gbits/s.

Initially, at power-up, coarse adjustment of the free running VCO frequency is required. This is achieved by the Frequency Window Detector (FWD) circuit. The FWD is a conventional frequency locked PLL.

The FWD checks the VCO frequency, which has to be within a 1000 ppm (parts per million) window around the desired frequency. The FWD then compares the divided VCO frequency (also available on pins PRSCLO and PRSCLOQ) with the reference frequency on pins CREF and CREFQ, usually 19.44 MHz. If the VCO frequency is found to be outside this window, the FWD disables the Data Phase Detector (DPD) and forces the VCO to a frequency within the window. As soon as the 'in window' condition occurs, which is visible on pin INWINDOW, the DPD starts acquiring lock on the incoming bit stream. Since the VCO frequency is very close to the expected bit rate, the phase acquisition will be almost instantaneous, resulting in quick phase lock to the incoming data stream.

Although the VCO is now locked to the incoming bit stream, the FWD is still supervising the VCO frequency and takes over control if the VCO drifts outside the predefined frequency window. This might occur during a 'loss of signal' situation. Due to the FWD, the VCO frequency is always close to the required bit rate, enabling rapid phase acquisition if the lost input signal returns.

Due to the loose coupling of 1000 ppm, the reference frequency does not need to be highly accurate or stable. Any crystal-based oscillator that generates a reasonably accurate frequency (e.g. 100 ppm) will do.

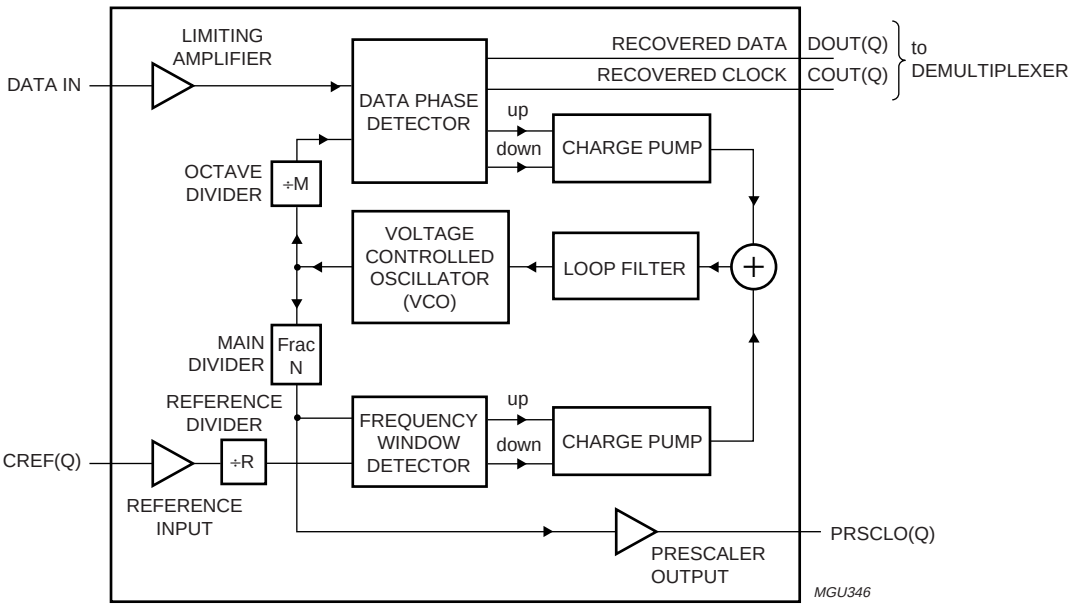


Fig.5 Block diagram of data and clock recovery.

Fractional N synthesizer

The DCR section has a fractional N synthesizer as frequency acquisition aid for the A-rate functionality. This allows the DCR to synchronize on incoming data, regardless of its bit rate. Any combination of bit rate and reference frequency is possible, due to the 22 bits fractional N synthesizer, allowing approximately 10 Hz frequency resolution. The LSB (bit K0) should be set to logic 1 to avoid limit cycles (cycles of less than maximum length). This leaves 21 bits (K<21:1>) available for free programming.

Programming the DCR

Programming the DCR involves four dividers; the reference frequency divider R, the main divider N, fractional divider K and the octave divider M. The first step is to determine in which octave the desired bit rate fits, see Tables 6 and 7.

The value for R is usually 1; see Section "Programming the reference clock" for detailed information.

Once the octave and the reference frequency are known, the main division ratio N and the fractional part K can be calculated according to the flowchart given in Fig.7.

Table 6 List of most common optical transmission protocols

PROTOCOL	BIT RATE (Mbits/s)	OCTAVE
10GE	3125.00	0
2xHDTV	2970.00	0
STM16/OC48 +FEC	2666.06	0
STM16/OC48	2488.32	0
DV-6000	2380.00	0
Fibre Channel	2125.00	0
HDTV	1485.00	1
D-1 Video	1380.00	1
DV-6010	1300.00	1
Gigabit Ethernet	1250.00	1
Fibre Channel	1062.50	1
OptiConnect	1062.50	1
ISC	1062.50	1
STM4/OC12	622.08	2
DV-6400	595.00	2
Fibre Channel	425.00	3
OptiConnect	265.63	3
Fibre Channel	212.50	4
ESCON/SBCON	200.00	4
STM1/OC3	155.52	4
FDDI	125.00	4
Fast Ethernet	125.00	4
Fibre Channel	106.25	5

Table 7 Octave definition

OCTAVE	M	LOWEST BIT RATE (Mbits/s)	HIGHEST BIT RATE (Mbits/s)
0	1	1800	3200
1	2	900	1800
2	4	450	900
3	8	225	450
4	16	112.5	225
5	32	56.25	112.5
6	64	28.125	56.25

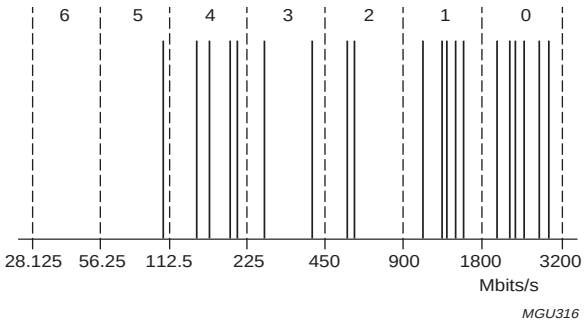


Fig.6 Commonly used line rates and allocation of octaves along a logarithmic bit rate scale.

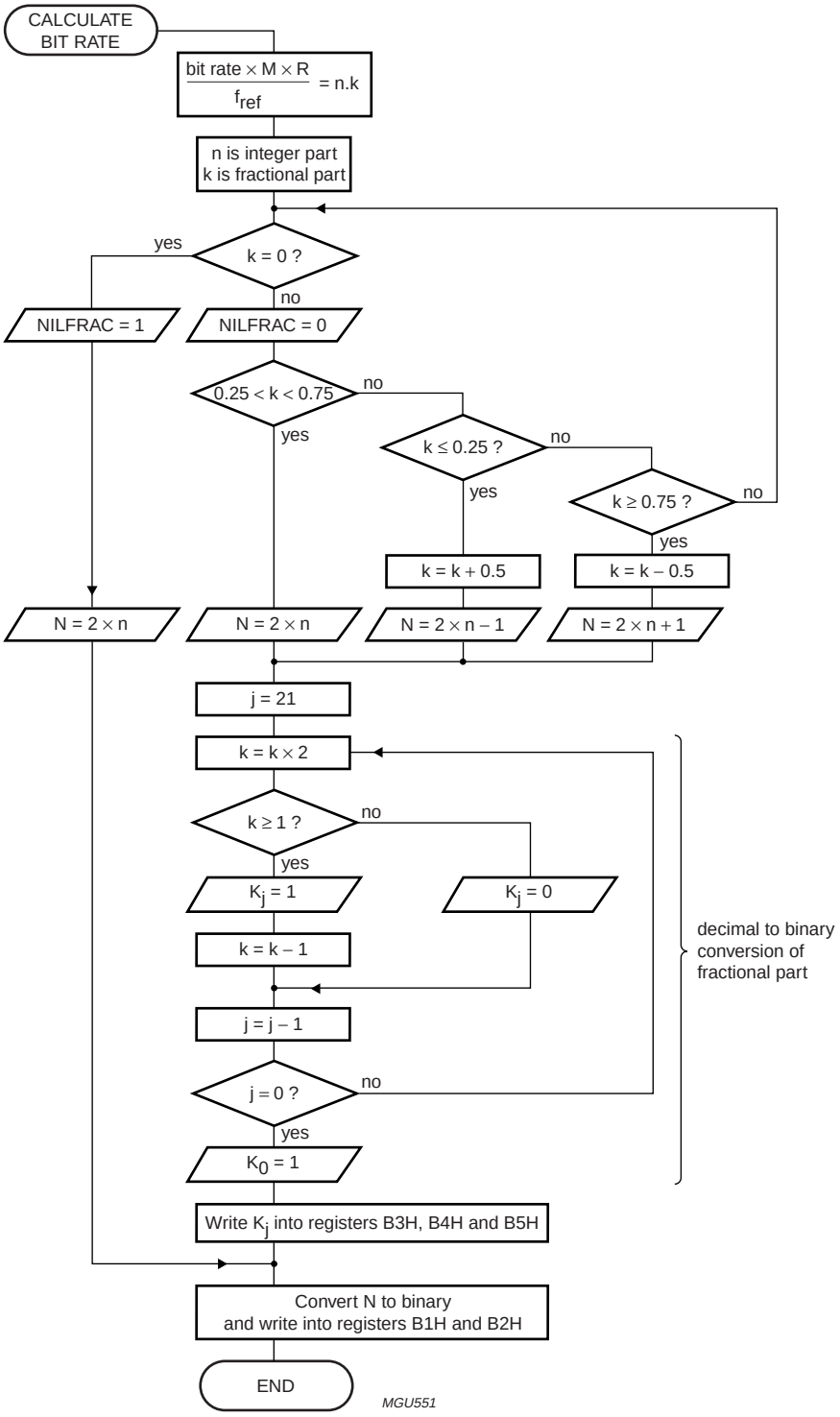


Fig.7 Flowchart for calculating N and K.

Example 1: An SDH or SONET link has a bit rate of 2488.32 Mbits/s (STM16/OC48) and consequently fits in octave number 0, so M = 1. Suppose the reference frequency provided at pins CREF(Q) is 77.76 MHz. This means that the reference division R needs to be 4. The values of n and k can be calculated from the flowchart:

$$n.k = \frac{\text{bit rate} \times M \times R}{f_{ref}} = \frac{2488.32\ \text{Mbits} \times 1 \times 4}{77.76\ \text{MHz}} = 128$$

Since k = 0 in this example, no fractional functionality is required, bit NILFRAC should be logic 1 (register B3H). N = 2 × n and no correction is required. Consequently the appropriate values are: R = 4 (register B6H), M = 1 (register B0H) and N = 256 (registers B1H and B2H).

Example 2: An SDH STM16 or SONET OC48 link with FEC has a bit rate of 2666.057143 Mbits/s (15/14 × 2488.32 Mbits/s) and consequently fits in octave number 0, so M = 1. Suppose the reference frequency provided at pins CREF(Q) is 38.88 MHz. This means that the reference division R, needs to be 2. The values of n and k can be calculated from the flowchart:

$$n.k = \frac{\text{bit rate} \times M \times R}{f_{ref}} = \frac{2666.05714283\ \text{Mbits} \times 1 \times 2}{38.88\ \text{MHz}} = 137.1428571$$

This means that n = 137, k = 0.1428571 and bit NILFRAC should be logic 0 (register B3H). Since k < 0.25, k is corrected to 0.6428571, while the corrected N becomes N = 273. Consequently the appropriate values are: R = 2 (register B6H), M = 1 (register B0H), N = 273 (registers B1H and B2H) and K = 10 1001 0010 0100 1001 0011 (registers B3H, B4H and B5H). The FEC bit rate is usually quoted to be 2666.06 Mbits/s. Due to round off errors, this leads to a slightly different value for k than in the example.

Example 3: A Fibre Channel link has a bit rate of 1062.50 Mbits/s and consequently fits in octave number 1, so M = 2. Suppose the reference frequency provided at pins CREF(Q) is 19.44 MHz. This means that the reference division R needs to be 1. The values of n and k can be calculated from the flowchart:

$$n.k = \frac{\text{bit rate} \times M \times R}{f_{ref}} = \frac{1062.50\ \text{Mbits} \times 2 \times 1}{19.44\ \text{MHz}} = 109.3106996$$

This means that n = 109, k = 0.3107 and bit NILFRAC should be logic 0 (register B3H). Since k is between 0.25 and 0.75, k does not need to be corrected and N = 2 × n = 218. Consequently the appropriate values are: R = 1 (register B6H), M = 2 (register B0H) and N = 218 (registers B1H and B2H). K = 01 0011 1110 0010 1000 0001 (registers B3H, B4H and B5H).

Example 4: A non standard transmission link has a bit rate of 3012 Mbits/s and consequently fits in octave number 0, so M = 1. Suppose the reference frequency provided at pins CREF(Q) is 20.50 MHz. This means that the reference division R needs to be 1. The values of n and k can be calculated from the flowchart:

$$n.k = \frac{\text{bit rate} \times M \times R}{f_{ref}} = \frac{3012\ \text{Mbits} \times 1 \times 1}{20.50\ \text{MHz}} = 146.9268293$$

This means that n = 146, k = 0.9268293 and bit NILFRAC should be logic 0 (register B3H). Since k is larger than 0.75, k needs to be corrected to 0.4268293 and N = 2 × n + 1 = 293. Consequently the appropriate values are: R = 1 (register B6H), M = 1 (register B0H) and N = 293 (registers B1H and B2H). K = 01 1011 0101 0001 0010 1011 (registers B3H, B4H and B5H).

If the I^2C-bus is not used, the DCR can be set up for the eight pre-programmed bit rates by pins DR0, DR1 and DR2 with an applied reference frequency of 19.44 MHz (see Table 3).

Programming the reference clock

Pre-programmed operation requires the use of any reference frequency between 18 and 21 MHz connected to pins CREF(Q). Pre-programmed operation in an SDH/SONET application requires the use of a 19.44 MHz reference clock, see Table 3.

In I²C-bus control mode, 4 ranges of clock frequencies can be used by programming R through bits REFDIV in register B6H; see Table 8. Internally, the reference frequency is always divided to the lowest range, from 18 to 21 MHz.

Table 8 Truth table for bits REFDIV

REFDIV	DIVISION FACTOR R	SDH/SONET REFERENCE FREQUENCY	REFERENCE FREQUENCY RANGE
00	1	19.44 MHz	18...21 MHz
01	2	38.88 MHz	36...42 MHz
10	4	77.76 MHz	72...84 MHz
11	8	155.52 MHz	144...168 MHz

Prescaler outputs

The prescaler output PRSCLO(Q) is the VCO frequency divided by the main division factor. It can be used as an accurate reference for another PLL, since it corresponds to the recovered data rate. If needed, the polarity of the prescaler outputs can be inverted by bit PRSCLOINV from register CBH.

If no prescaler information is desired, the output can be disabled by bit PRSCLOEN from the same register. Apart from these settings, the type of output, the termination mode and the signal amplitude can be set. These parameters follow the settings of the parallel demultiplexer outputs. For programming details, see Section “Configuring the parallel bus”.

Programming the FWD

The default width of the window for frequency acquisition is 1000 ppm around the desired bit rate. This window size can be changed between 4000 and 250 ppm by I²C-bus bits WINDOWSIZE from I²C-bus register B6H. This allows for loose or tight coupling of the VCO to the applied reference clock. Another feature is to define a window width of 0 ppm, by means of pin WINSIZE (pin 13). This effectively removes the dead zone from the FWD, rendering the FWD into a classical PLL.

The VCO will be directly locked to the reference signal instead of the incoming bit stream. Apart from pin WINSIZE, this mode can be invoked by I²C-bus bits I2CWINSIZE and WINSIZE from I²C-bus register B6H.

Table 9 Truth table for pin WINSIZE

WINSIZE	FREQUENCY WINDOW
LOW	0 ppm
HIGH	1000 ppm

Accurate clock generation during loss of signal, bit AUTOWIN

A zero window size is especially interesting in the absence of input data, since the frequency of the recovered clock will be equal to the reference frequency including its tolerance.

The option AUTOWIN makes the window size dependent on the LOS status of the active limiter channel. If the optical input signal is lost, the FWD automatically selects the 0 ppm window size; i.e. direct lock on to the reference frequency. This results is a stable and defined output clock during ‘loss of signal’ situations, while automatically reverting back to normal DCR operation when the input signal returns.

The accuracy of the reference frequency needs to be better than 20 ppm if the application is to comply with ITU-T recommendations.

INWINDOW signal

The status of the FWD circuit is reflected in the state of pin INWINDOW; HIGH for an ‘in window’ situation and LOW whenever the VCO is outside the defined frequency window.

Jitter performance

The TZA3012AHW has been optimized for best jitter tolerance performance. For all SDH/SONET bit rates, the jitter tolerance exceeds compliance with ITU-T standard G.958.

Demultiplexer

The demultiplexer converts the serial input bit stream to parallel format (1 : 16, 1 : 10, 1 : 8, 1 : 4). The output data is available on a scalable bus, of which the output driver type can be either LVPECL or CML. Apart from the deserializing function, the demultiplexer comprises a parity calculator and a frame header detection circuit. The calculated parity, EVEN, is output at pins PARITY and PARITYQ, whereas occurrence of the frame header pattern in the data stream results in a 1 clock cycle wide pulse on outputs FP and FPQ.

If ENBA is HIGH, automatic byte (word) alignment takes place, formatting the parallel output to logical bytes or words. Apart from pin ENBA, this mode can be invoked by I²C-bus bits I2CENBA and ENBA from I²C-bus register A8H.

To support most commonly used transmission systems and protocols, the demultiplexing ratio can be set and the frame header pattern programmed to any 32 or 10-bit pattern (see Section “Frame detection”).

If required, the demultiplexer output can be forced into a fixed logic state by the mute function.

Adjustable demultiplexing ratio

The demultiplexing ratio of the TZA3012AHW can be configured by pins DMXR0 and DMXR1 or bits DMXR of I²C-bus register DMXCNF (I²C-bus register A8H), according to Table 10.

Bit I2CDMXR of register A8H enables programming of the demultiplexing ratio by the bits DMXR.

The parallel output bus is always centred around the middle (V_{EE}, pin 63) for optimum layout connectivity. Table 10 lists the active outputs for the various demultiplexing ratios. In I²C-bus mode, the 1 : 16 ratio is default. The LSB appears on the output with the lowest pin number.

The bus order can be changed with I²C-bus bit BUSSWAP in register DMXCNF (A8H). Bit BUSSWAP reverses the order of bits from MSB to LSB or vice versa, to allow for optimal layout connectivity.

The highest supported parallel bus speed is 400 Mbits/s. Therefore, the 1 : 4 demultiplexing ratio is only supported for bit rates up to 1.6 Gbits/s.

Table 10 Setting the demultiplexing ratio

DMXR1 (PIN)	DMXR0 (PIN)	DMXR (REG A8H)	DEMULTIPLEXING RATIO	ACTIVE OUTPUTS	ACTIVE OUTPUT PINS LSB...MSB
LOW	LOW	00	1 : 4	D06...D09	59...67
LOW	HIGH	01	1 : 8	D04...D11	55...71
HIGH	LOW	10	1 : 10	D03...D12	53...73
HIGH	HIGH	11	1 : 16	D00...D15 (all)	44...82

Frame detection

Byte alignment is enabled if the Enable Byte Alignment (ENBA) input is HIGH. Whenever a 32-bit or 10-bit sequence matches the programmed header pattern, the incoming data is formatted into logical bytes or words and a frame pulse is generated on differential outputs FP and FPQ. Any header pattern can be programmed through I²C-bus registers HEADER0 to HEADER3. It is possible to enter a “don’t care” for any bit position, e.g. to program a header pattern that is much shorter than 32 or 10 bits or to program a pattern with a gap in it.

For this, it is necessary to program I²C-bus registers HEADERX0 to HEADERX3, as in the example shown in Fig.8.

The contents of the don’t care I²C-bus registers serve as a masking pattern on top of the programmed framing pattern.

The default frame header pattern is F6F62828H, corresponding to the middle section of the standard SDH/SONET frame header (the last two A1 bytes plus the first two A2 bytes).

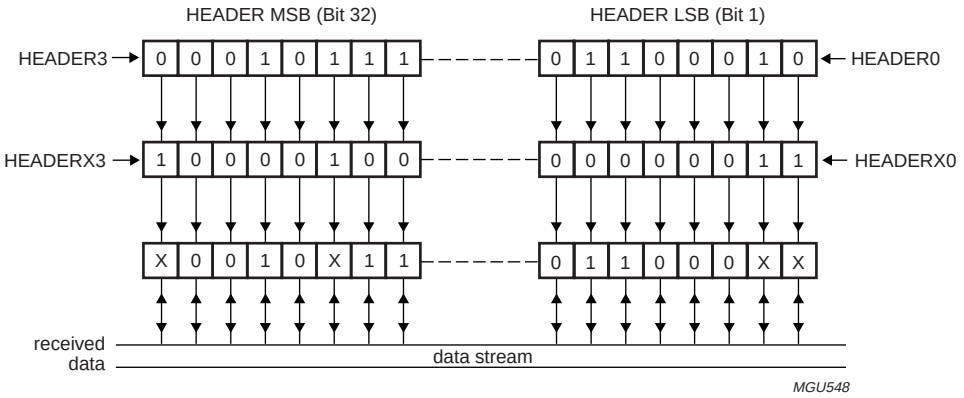


Fig.8 Example of programming the framing pattern: the symbol ‘X’ represents a “don’t care”.

If ENBA is LOW, no active alignment takes place. However, if the framing pattern happens to occur in the formatted data, a frame pulse will still be output on pins FP and FPQ.

For 10-bit oriented protocols, such as Gigabit Ethernet, the frame header detection works on a 10-bit pattern sequence. These 10 bits should be programmed into I^2C-bus registers HEADER3 and HEADER2 (two LSBs only), the remaining 22 bits are ignored. Again, a ‘don’t care’ pattern overlay can be programmed in I^2C-bus registers HEADERX3 and HEADERX2 (two bits).

Since some 10-bit oriented protocols use a DC balancing code, the detection pattern could appear in complementary form in the data stream. By setting bit CMPL in I^2C-bus register DMXCNF (A8H), the header detection will scan the data stream for the programmed pattern as well as its complement simultaneously. Therefore, either occurrence will result in a ‘byte’ alignment and a corresponding frame pulse on pins FP and FPQ.

The default pattern (after power-up) is ‘0011111010b’ or K28.5 character plus alternating 010. This is the only pattern containing five consecutive bits of the same sign.

Receiver framing in SDH/SONET applications

Figure 9 shows a typical SDH/SONET reframe sequence involving byte alignment. Frame and byte boundary detection is enabled on the rising edge of ENBA and remains enabled while ENBA is HIGH. Boundaries are recognized on receipt of the second A2 byte and FP goes HIGH for one POCLK cycle.

In 1 : 16 mode, the first two A2 bytes in the frame header are the first data word to be reported with the correct alignment on the outgoing data bus (D00 to D15). In 1 : 8 mode the first A2 byte is the first aligned data byte (D04 to D11), while in 1 : 4 mode the most significant nibble of the first A2 byte is the first aligned data (D06 to D09).

When interfacing with a section terminating device, ENBA must remain HIGH for a full frame after the initial frame pulse. This is to allow the section terminating device to verify internally that frame and byte alignment are correct (see Fig.10). Byte boundary detection is disabled on the first FP pulse after ENBA has gone LOW.

Figure 11 shows frame and byte boundary detection activated on the rising edge of ENBA, and deactivated by the first FP pulse after ENBA has gone LOW.

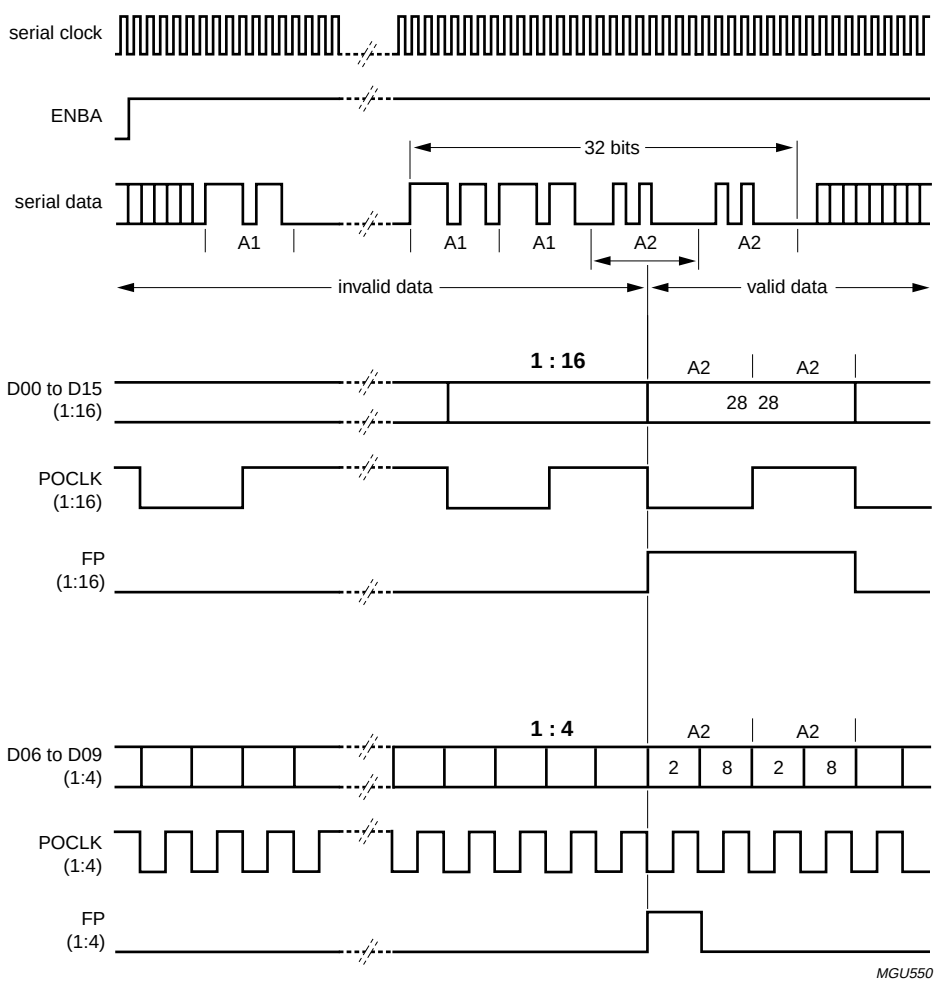


Fig.9 Frame and byte detection in SDH/SONET application.

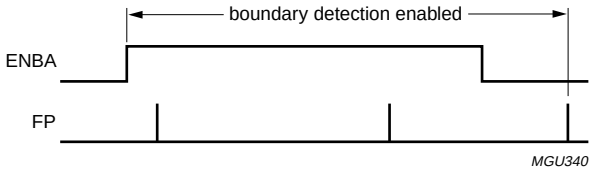


Fig.10 ENBA timing with section terminating device.

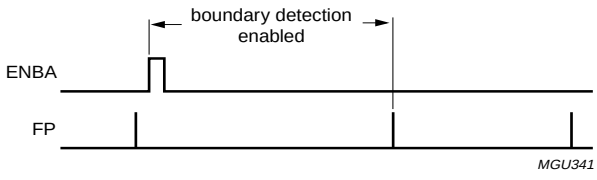


Fig.11 Alternate ENBA timing.

Parity generation

Outputs PARITY(Q) provide the EVEN parity of the byte/word that is currently available on the parallel bus. With bit PARINV of I²C-bus register C9H, the parity can be made ODD. If no parity is required, I²C-bus bit PAREN can disable this output, to reduce power dissipation.

Configuring the parallel bus

Several options exist that allow flexible configuration of the parallel bus and associated outputs. The options for POCLK(Q), D00(Q) to D15(Q), FP(Q), PARITY(Q) and PRSCLO(Q) are: output driver type, termination mode, output amplitude, signal polarity, bits order, mute and selective enabling or disabling. These options are set in registers DMXCNF (A8H), IOCNF (C9H) and IOCNF3 (C8H).

Bit MFOUTMODE selects the CML or LVPECL output driver (default LVPECL). Bit MFOUTTERM sets the termination mode, standard LVPECL or floating termination, or in case of CML, DC or AC coupled. The four MFS bits adjust the amplitude in all cases. I²C-bus bit PDEN disables the output driver. This is not the same as the MUTE option, which forces a logic 0 state. The default output amplitude is 800 mV (p-p) single-ended.

Bit PDINV inverts the polarity of the parallel data, POCLKINV inverts the clock, effectively shifting the clock edge by half a clock cycle, and changing the rising edge to a falling edge. This might resolve a parallel bus timing problem. The bus clock can even be disabled by I²C-bus bit POCLKEN. The same features, with other I²C-bus bits, hold for FP and FPQ and the parity outputs PARITY and PARITYQ.

Loop mode I/Os

The “diagnostic loop back” is activated by setting pin ENLINQ to LOW. In this case, the demultiplexer will select inputs DLOOP(Q) and CLOOP(Q) instead of taking the input from the DCR. The “line loop back” mode is activated by setting ENLOUTQ to LOW. In this case the recovered clock and serial data will be available at output pins DOUT(Q) and COUT(Q).

Configuring the RF I/Os

The polarity of the individual serial data and clock I/Os can be inverted via the I²C-bus. The position of the data and clock outputs (or inputs) can be swapped. This solves connectivity problems with other ICs. Registers IOCNF0 (CBH) and IOCNF1 (CAH) program all RF I/O configurations.

When the RF input data and clock are swapped by means of bit CDINSWAP (register CAH), the signals present at pins CLOOP(Q) are assumed to be data and the signals at pins DLOOP(Q) are assumed to be clock. The same holds for swapping the RF outputs. Data is output at pins COUT(Q) and clock at pins DOUT(Q).

The RF CML outputs have an adjustable signal amplitude from 60 mV (p-p) to 1000 mV (p-p) (single-ended) in 16 steps, by bits RFS and RFSWING (register CBH). The default amplitude is 80 mV (p-p) single-ended. The termination scheme is AC coupled.

CMOS control inputs

Most CMOS control inputs have an internal pull-up resistor. An open circuit equals a HIGH input. Only the LOW state needs to be actively forced. This holds for pins UI, INSEL, WINSIZE, DMXR0, DMXR1, ENBA, ENLOUTQ, ENLINQ and CS. The same is true for pins DR0, DR1 and DR2 in pre-programmed mode (UI = LOW). In I²C-bus mode (UI = HIGH), pins SCL and SDA comply with the I²C-bus interface standard.

Power supply connections

Four separate supply domains (V_{DD}, V_{CCD}, V_{CCO}, and V_{CCA}) provide isolation between the various functional blocks. Each supply domain should be connected to a common V_{CC} via separate filters. **All supply pins, including the exposed die pad, must be connected**. The die pad should be connected with the lowest inductance possible. Since the die pad is also used as the main ground return of the chip, the connection should have a low DC impedance as well. The voltage supply levels should be in accordance with the values specified in Chapters “Characteristics” and “Limiting values”.

All external components should be surface mounted devices, preferably of size 0603 or smaller. The components must be mounted as closely to the IC as possible.

Interrupt controler

The configurable interrupt controler is based on five status flags:

- Loss of signal on channel 1
- Loss of signal on channel 2
- DCR in window indication
- Switching of limiters indication
- Temperature alarm.

This controler contains three I²C-bus registers, namely interrupt register (address 00H), status register (address 01H), and mask register (address CCH). In the I²C-bus status register the history is stored, the reason for an interrupt. The status register shows the present status of the receiver. The mask register determines the masking of the flags generating an interrupt on pin INT.
See Tables 12, 13 and 29.

The MSB of I²C-bus register INTMASK determines the output type of pin INT: standard CMOS output or open-drain output. The latter is the default value, which provides for multiple receivers sharing a common interrupt signal wire, with a 3.3 kΩ pull-up resistor (INT is active LOW in this case). The polarity of the INT output can be inverted by bit INTPOL from register CCH.

The interrupt and status register can be polled by an I²C-bus read action. After the read action the interrupt register is reset by clearing all interrupt flags. If the ’alarm‘ is still present, the flag is immediately set again in the I²C-bus interrupt register.

The I²C-bus status register is not reset since it always shows the present status of the receiver.

I²C-bus registers

Setting pin UI HIGH or leaving the pin open allows I²C-bus programming. The I²C-bus registers can be accessed via the 2-wire I²C-bus interface, pins SCL and SDA, if CS (chip select) is HIGH during read or write actions. Table 11 shows the I²C-bus register list.

Table 11 I²C-bus register list

ADDRESS	NAME	FUNCTION	DEFAULT	RANGE
00H	INTERRUPT	interrupt register (see Table 12)		n.a.
01H	STATUS	status register (see Table 13)		n.a.
A0H	HEADER3	programmable header, MSB 1 : 10 ratio	1111 0110 0011 1110	n.a.
A1H	HEADER2	programmable header 1 : 10 ratio	1111 0110 10xx xxxx	n.a.
A2H	HEADER1	programmable header	0010 1000	n.a.
A3H	HEADER0	programmable header, LSB	0010 1000	n.a.
A4H	HEADERX3	programmable header don't care, MSB 1 : 10 ratio	0000 0000 0000 0000	n.a.
A5H	HEADERX2	programmable header don't care 1 : 10 ratio	0000 0000 0000 0000	n.a.
A6H	HEADERX1	programmable header don't care	0000 0000	n.a.
A7H	HEADERX0	programmable header don't care, LSB	0000 0000	n.a.
A8H	DMXCNF	demultiplexer configuration register (see Table 14)	0000 1011	n.a.
B0H	DIVCNF	octave and loop mode configuration register (see Table 15)	0000 0000	n.a.
B1H	MAINDIV1	main divider division ratio N (MSB) (see Table 16)	0000 0001	[128 to 511]
B2H	MAINDIV0	main divider division ratio N (see Table 17)	0000 0000	
B3H	FRACN2	fractional divider division ratio K (see Table 18)	1000 0000	n.a.
B4H	FRACN1	fractional divider division ratio K (see Table 19)	0000 0000	n.a.
B5H	FRACN0	fractional divider division ratio K (see Table 20)	0000 0000	n.a.
B6H	DCRCNF	DCR configuration register (see Table 21)	0000 1100	n.a.
BCH	LIMLOS1TH	limiter 1 loss of signal threshold register	0000 0000	[0 to 255]
BDH	LIMLOS1CNF	limiter 1 loss of signal configuration register (see Table 22)	0000 1101	n.a.
BEH	LIMLOS2TH	limiter 2 loss of signal threshold register	0000 0000	[0 to 255]
BFH	LIMLOS2CNF	limiter 2 loss of signal configuration register (see Table 23)	0000 1101	n.a.
C0H	LIMSLICE1	limiter 1 slice level register	0000 0000	[0 to 255]
C1H	LIMSLICE2	limiter 2 slice level register	0000 0000	[0 to 255]
C2H	LIMCNF	limiter configuration register (see Table 24)	0000 1000	n.a.
C8H	IOCNF3	I/O configuration register 3; parallel outputs (see Table 25)	0000 1100	n.a.
C9H	IOCNF2	I/O configuration register 2; parallel outputs (see Table 26)	1010 1010	n.a.
CAH	IOCNF1	I/O configuration register 1; RF serial I/Os (see Table 27)	0000 0000	n.a.
CBH	IOCNF0	I/O configuration register 0; RF serial I/Os (see Table 28)	0010 0011	n.a.
CCH	INTMASK	interrupt masking register (see Table 29)	0101 0000	n.a.

Table 12 Register INTERRUPT (address: 00H)

BIT								PARAMETER	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**DESCRIPTION**	**NAME**
								Loss Of Signal (LOS) on channel 1	LOS1
							1	no signal present (loss of signal condition)	
							0	signal present	
								Loss Of Signal (LOS) on channel 2	LOS2
						1		no signal present (loss of signal condition)	
						0		signal present	
								DCR frequency indication	INWINDOW
					1			frequency outside predefined window (unlocked)	
					0			frequency inside predefined window (locked)	
								switching of limiters indication	LIMSEL
				1				indication of switching from one limiter to the other	
				0				no switching	
								temperature alarm	TALARM
			1					junction temperature ≥130 °C	
			0					junction temperature <130 °C	
0	0	0							reserved

Table 13 Register STATUS (address: 01H)

BIT								PARAMETER	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**DESCRIPTION**	**NAME**
								Loss Of Signal (LOS) on channel 1	LOS1
							1	no signal present (loss of signal condition)	
							0	signal present	
								Loss Of Signal (LOS) on channel 2	LOS2
						1		no signal present (loss of signal condition)	
						0		signal present	
								DCR frequency indication	INWINDOW
					1			frequency inside predefined window (locked)	
					0			frequency outside predefined window (unlocked)	
								limiter autoselect indication	LIMSEL
				1				limiter 1 active	
				0				limiter 2 active	
								temperature alarm	TALARM
			1					junction temperature ≥130 °C	
			0					junction temperature <130 °C	
0	0	0							reserved

Table 14 Register DMXCNF (address: A8H, default value: 0BH; see also last row of table)

BIT								PARAMETER	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**DESCRIPTION**	**NAME**
								demultiplexing ratio	DMXR
						1	1	1 : 16	
						1	0	1 : 10	
						0	1	1 : 8	
						0	0	1 : 4	
								demultiplexing ratio programming	I2CDMXR
					1			through I^2C-bus interface	
					0			through external pins DMXR0 and DMXR1	
								header detection in 1 : 10 Gigabit Ethernet mode	CMPL
				1				simultaneously check for complementary header	
				0				check programmed header only	
								parallel bus swapping	BUSSWAP
			1					D00 = MSB, D15 = LSB (swapped)	
			0					D15 = MSB, D00 = LSB (normal)	
								demultiplexer mute parallel outputs	DMXMUTE
		1						mute; parallel outputs forced to logic 0	
		0						no mute	
								enable byte alignment	ENBA
	1							byte alignment enabled	
	0							byte alignment disabled	
								ENBA control	I2CENBA
1								through I^2C-bus interface	
0								through external pin ENBA	
0	0	0	0	1	0	1	1		default value

Table 15 Register DIVCNF (address: B0H, default value: 00H; see also last row of table)

BIT								PARAMETER	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**DESCRIPTION**	**NAME**
								division ratio octave divider M; octave selection	DIV_M
					0	0	0	M = 1, octave no. 0	
					0	0	1	M = 2, octave no. 1	
					0	1	0	M = 4, octave no. 2	
					0	1	1	M = 8, octave no. 3	
					1	0	0	M = 16, octave no. 4	
					1	0	1	M = 32, octave no. 5	
					1	1	0	M = 64, octave no. 6	
			0	0					reserved
								enable loop mode inputs	ENLOOPIN
		1						loop mode inputs enabled	
		0						loop mode inputs disabled	
								enable loop mode outputs	ENLOOPOUT
	1							loop mode outputs enabled	
	0							loop mode outputs disabled	
								loop mode control	I2CLOOPMODE
1								through I^2C-bus interface	
0								through external pins ENLINQ and/or ENLOUTQ	
0	0	0	0	0	0	0	0		default value

Table 16 Register MAINDIV1 (address: B1H, default value: 01H; see also last row of table)

BIT								PARAMETER	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**DESCRIPTION**	**NAME**
							N8	division ratio divider, N; N8 = MSB	DIV_N
0	0	0	0	0	0	0	1		default value

Table 17 Register MAINDIV0 (address: B2H, default value: 00H; see also last row of table)

BIT								PARAMETER	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**DESCRIPTION**	**NAME**
N7	N6	N5	N4	N3	N2	N1	N0	division ratio divider, N; N0 = LSB	DIV_N
0	0	0	0	0	0	0	0		default value

Table 18 Register FRACN2 (address: B3H, default value: 80H; see also last row of table)

BIT								PARAMETER	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**DESCRIPTION**	**NAME**
NF	x	K21	K20	K19	K18	K17	K16	fractional divider, K; K21 = MSB	DIV_K
1 0								NILFRAC control bit (NF) no fractional N functionality fractional N functionality	NILFRAC
1	0	0	0	0	0	0	0		default value

Table 19 Register FRACN1 (address: B4H, default value: 00H; see also last row of table)

BIT								PARAMETER	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**DESCRIPTION**	**NAME**
K15	K14	K13	K12	K11	K10	K9	K8	fractional divider, K	DIV_K
0	0	0	0	0	0	0	0		default value

Table 20 Register FRACN0 (address: B5H, default value: 00H; see also last row of table)

BIT								PARAMETER	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**DESCRIPTION**	**NAME**
K7	K6	K5	K4	K3	K2	K1	K0	fractional divider, K; K0 = LSB	DIV_K
0	0	0	0	0	0	0	0		default value

Table 21 Register DCRCNF (address: B6H, default value: 0CH; see also last row of table)

BIT								PARAMETER	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**DESCRIPTION**	**NAME**
								frequency window size, relative to bit rate	WINDOWSIZE
					0	1	0	4000 ppm	
					0	1	1	2000 ppm	
					1	0	0	1000 ppm	
					1	0	1	500 ppm	
					1	1	0	250 ppm	
				1				manual frequency window size selection window size according to 'WINDOWSIZE' (default value 1000 ppm); PLL frequency loosely coupled to reference crystal	WINSIZE
				0				window size = 0 ppm; PLL frequency directly synthesized from reference crystal	
								WINSIZE control bit	I2CWINSIZE
			1					through I^2C-bus interface	
			0					through external pin WINSIZE	
								automatic frequency window size selection	AUTOWIN
		1						enabled	
		0						disabled	
								reference frequency divider	REFDIV
1	1							R = 8; reference frequency = 155.52 MHz	
1	0							R = 4; reference frequency = 77.76 MHz	
0	1							R = 2; reference frequency = 38.88 MHz	
0	0							R = 1; reference frequency = 19.44 MHz	
0	0	0	0	1	1	0	0		default value

Table 22 Register LIMLOS1CNF (address: BDH, default value: 0DH; see also last row of table)

BIT								PARAMETER	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**DESCRIPTION**	**NAME**
								loss of signal detection on channel 1	LOS1
							1	LOS detection enabled	
							0	LOS detection disabled	
								loss of signal threshold level control bit channel 1	I2CREFLVL1
						1		through I^2C-bus interface by internal DAC; register BCH	
						0		through analog voltage on pin LOSTH1	
								loss of signal detection hysteresis channel 1	HYS1
			0	0	0			0 dB	
			0	0	1			0.85 dB	
			0	1	0			1.7 dB	
			0	1	1			2.5 dB	
			1	0	0			3.4 dB	
			1	0	1			4.2 dB	
			1	1	0			5.1 dB	
			1	1	1			6 dB	
								slice level of channel 1	SL1
		1						slice level enabled	
		0						slice level disabled	
								slice level sign of channel 1	SL1SGN
	1							positive slice level	
	0							negative slice level	
								polarity of LOS channel 1	LOS1POL
1								inverted polarity	
0								normal polarity	
0	0	0	0	1	1	0	1		default value

Table 23 Register LIMLOS2CNF (address: BFH, default value: 0DH; see also last row of table)

BIT								PARAMETER	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**DESCRIPTION**	**NAME**
								loss of signal detection on channel 2	LOS2
							1	LOS detection enabled	
							0	LOS detection disabled	
								loss of signal threshold level control bit channel 2	I2CREFLVL2
						1		through I^2C-bus interface by internal DAC; register BEH	
						0		through analog voltage on pin LOSTH2	
								loss of signal detection hysteresis channel 2	HYS2
			0	0	0			0 dB	
			0	0	1			0.85 dB	
			0	1	0			1.7 dB	
			0	1	1			2.5 dB	
			1	0	0			3.4 dB	
			1	0	1			4.2 dB	
			1	1	0			5.1 dB	
			1	1	1			6 dB	
								slice level of channel 2	SL2
		1						slice level enabled	
		0						slice level disabled	
								slice level sign of channel 2	SL2SGN
	1							positive slice level	
	0							negative slice level	
								polarity of LOS channel 2	LOS2POL
1								inverted polarity	
0								normal polarity	
0	0	0	0	1	1	0	1		default value

Table 24 Register LIMCNF (address: C2H, default value: 08H; see also last row of table)

BIT								PARAMETER	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**DESCRIPTION**	**NAME**
								amplifier octave selection	AMPOCT
					0	0	0	octave no. 0; 1800 to 3200 Mbits/s	
					0	0	1	octave no. 1; 900 to 1800 Mbits/s	
					0	1	0	octave no. 2; 450 to 900 Mbits/s	
					0	1	1	octave no. 3; 225 to 450 Mbits/s	
					1	x	x	octave no. 4; 30 to 225 Mbits/s	
								limiter channel selection	INSEL
				1				channel 1 active	
				0				channel 2 active	
								limiter channel selection control bit	I2CINSEL
			1					through I^2C-bus interface; bit INSEL	
			0					through external pin INSEL	
								single/dual limiter selection	BOTHON
		1						both channels active	
		0						single channel active, according to INSEL	
0	0								reserved
0	0	0	0	1	0	0	0		default value

Table 25 Register IOCNF3 (address: C8H, default value: 0CH; see also last row of table)

BIT								PARAMETER	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**DESCRIPTION**	**NAME**
								parallel output signal amplitude	MFS
				0	0	0	0	0 mV (p-p)	
				0	0	0	1	minimum signal level; 120 mV (p-p)	
				1	1	0	0	default signal level; 800 mV (p-p)	
				1	1	1	1	maximum signal level; 1000 mV (p-p)	
		0	0						reserved
								parallel output termination	MFOUTTERM
	1							LVPECL mode: floating, CML mode: AC coupled	
	0							LVPECL mode: standard, CML mode: DC coupled	
								parallel output mode	MFOUTMODE
1								CML; Current Mode Logic	
0								LVPECL; Positive Emitter Coupled Logic	
0	0	0	0	1	1	0	0		default value

Table 26 Register IOCNF2 (address: C9H, default value: AAH; see also last row of table)

BIT								PARAMETER	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**DESCRIPTION**	**NAME**
								parallel data output polarity	PDINV
							1	inverted	
							0	normal	
								parallel data output enable	PDEN
						1		enabled	
						0		disabled	
								parallel clock output polarity	POCLKINV
					1			inverted	
					0			normal	
								parallel clock output enable	POCLKEN
				1				enabled	
				0				disabled	
								parity output polarity	PARINV
			1					inverted	
			0					normal	
								parity output enable	PAREN
		1						enabled	
		0						disabled	
								frame pulse output polarity	FPINV
	1							inverted	
	0							normal	
								frame pulse output enable	FPEN
1								enabled	
0								disabled	
1	0	1	0	1	0	1	0		default value

Table 27 Register IOCNF1 (address: CAH, default value: 00H; see also last row of table)

BIT								PARAMETER	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**DESCRIPTION**	**NAME**
								loop mode clock input polarity	CININV
							1	inverted	
							0	normal	
								loop mode data input polarity	DININV
						1		inverted	
						0		normal	
								loop mode input clock and data swap	CDINSWAP
					1			swapped clock and data input pairs	
					0			normal clock and data input	
								loop mode clock output polarity	COUTINV
				1				inverted	
				0				normal	
								loop mode data output polarity	DOUTINV
			1					inverted	
			0					normal	
								loop mode output clock and data swap	CDOUTSWAP
		1						swapped clock and data output pairs	
		0						normal clock and data output	
0	0								reserved
0	0	0	0	0	0	0	0		default value

Table 28 Register IOCNF0 (address: CBH, default value: 23H; see also last row of table)

BIT								PARAMETER	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**DESCRIPTION**	**NAME**
								RF serial output signal amplitude:	RFS
				0	0	0	0	minimum signal level; 60 mV (p-p)	
				0	0	1	1	default signal level; 250 mV (p-p)	
				1	1	1	1	maximum signal level; 1000 mV (p-p)	
								prescaler output polarity	PRSCLOINV
			1					inverted	
			0					normal	
								prescaler output enable	PRSCLOEN
		1						enabled	
		0						disabled	
								RF serial output swing	RFSWING
	1							high swing	
	0							low swing	
0									reserved
0	0	1	0	0	0	1	1		default value

Table 29 Register INTMASK (address: CCH, default value: A0H; see also last row of table)

BIT								PARAMETER	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**DESCRIPTION**	**NAME**
								mask LOS1 signal	MLOS1
							1	not masked	
							0	masked; note 1	
								mask LOS2 signal	MLOS2
						1		not masked	
						0		masked; note 1	
								mask INWINDOW signal	MINWINDOW
					1			not masked	
					0			masked; note 1	
								mask LIMSEL signal	MLIMSEL
				1				not masked	
				0				masked; note 1	
								mask Temperature Alarm	MTALARM
			1					not masked	
			0					masked; note 1	
		0							reserved
								INT polarity mode	INTPOL
	1							inverted	
	0							normal	
								INT output mode	INTOUT
1								standard CMOS output	
0								open-drain output	
0	1	0	1	0	0	0	0		default value

Note

1. Signal is not processed by the interrupt controller.

TZA3012AHW without using the I²C-bus

Although the TZA3012AHW is intended to be programmed via an I²C-bus, a lot of features can be accessed from external pins. This chapter lists the functions of the TZA3012AHW if the User Interface (UI) pin is LOW.

FEATURES WITHOUT THE I²C-BUS (UI = V_{EE}):

- 1 of 4 pre-programmed SDH/SONET bit rates; STM1/OC3, STM4/OC12, STM16/OC48, STM16/OC48 +FEC (DR2...DR0)
- 1 of 4 pre-programmed bit rates; Fibre Channel, double Fibre Channel, Gigabit Ethernet, 10-Gigabit Ethernet (DR2...DR0)
- 1 of 4 demultiplexing ratios; 1 : 16, 1 : 10, 1 : 8 or 1 : 4 (DMXR1 and DMXR0)
- Input channel selection (INSEL)
- Received signal strength indicator, independently for channels 1 and 2
- Loss of signal detection threshold for each input channel individually (LOSTH1 and LOSTH2)
- Automatic disable of unused logarithmic detector (LOSTH1 and LOSTH2)
- Loop mode serial input and output configuration (ENLINQ and ENLOUTQ)
- Automatic byte alignment for SDH/SONET or Gigabit Ethernet (ENBA)
- Frame detection for SDH/SONET (pattern is A1A1A2A2) or Gigabit Ethernet
- EVEN parity generation
- LVPECL parallel outputs with 800 mV (p-p) single-ended signal (DC coupled termination to V_{CC} – 2 V)
- CML serial RF outputs with typical 80 mV (p-p) single-ended signal (AC coupled load)
- In window detection (INWINDOW)
- Sizeable frequency window, 1000 ppm or 0 ppm (WINSIZE)
- Temperature alarm (pin INT; open-drain)
- Supported reference frequency from 18 to 21 MHz.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CCA}, V_{CCD}, V_{CCO}, V_{DD}	supply voltages	–0.5	+3.6	V
V_n	DC voltage on			
	pins D00 to D15, D00Q to D15Q, POCLK, POCLKQ, FP, FPQ, PARITY, PARITYQ, PRSCLO and PRSCLOQ	V_{CC} – 2.5	V_{CC} + 0.5	V
	pins LOSTH1, LOSTH2 and RREF	–0.5	V_{CC} + 0.5	V
	pins RSSI1 and RSSI2	–0.5	V_{CC} + 0.5	V
	pins UI, INSEL, WINSIZE, CS, SDA, SCL, DMXR0, DMXR1, ENBA, ENLOUTQ and ENLINQ	–0.5	V_{CC} + 0.5	V
	pins LOS1, LOS2 and INWINDOW	–0.5	V_{CC} + 0.5	V
	pin INT	–0.5	V_{CC} + 0.5	V
I_n	input current on			
	pins IN1, IN1Q, IN2 and IN2Q	–30	+30	mA
	pins CREF, CREFQ, CLOOP, CLOOPQ, DLOOP and DLOOPQ	–20	+20	mA
	pin INT	–2	+2	mA
T_{amb}	ambient temperature	–40	+85	°C
T_j	junction temperature	–40	+125	°C
T_{stg}	storage temperature	–65	+150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	notes 1 and 2	16	K/W

Notes

1. In compliance with JEDEC standards JESD51-5 and JESD51-7.
2. Four-layer Printed Circuit Board (PCB) in still air with 36 plated vias connected with the heatsink and the second and fourth layer in the PCB.

CHARACTERISTICS

V_{CC} = 3.14 to 3.47 V; T_{amb} = –40 to +85 °C; $R_{th(j-a)} \leq 16$ K/W; all characteristics are specified for the default settings (note 1); all voltages are referenced to ground; positive currents flow into the device; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
I_{CCA}	supply current (analog)		–	20	–	mA
I_{CCD}	supply current (digital)	see Figs 12 and 14	–	350	–	mA
I_{CCO}	supply current (oscillator)		–	25	–	mA
I_{DD}	supply current (digital)		–	5	–	mA
$I_{CC(tot)}$	total supply current		–	400	–	mA
P_{tot}	total power dissipation		–	1.3	–	W
CMOS input; pins UI, DR0, DR1, DR2, INSEL, WINSIZE, CS, DMXR0, DMXR1, ENBA, ENLOUTQ and ENLINQ						
V_{IL}	LOW-level input voltage		–	–	$0.3V_{CC}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{CC}$	–	–	V
I_{IL}	LOW-level input current	V_{IL} = 0 V	–	–	–200	μA
I_{IH}	HIGH-level input current	$V_{IH} = V_{CC}$	–	–	10	μA
CMOS output; pins LOS1, LOS2, INWINDOW and INT						
V_{OL}	LOW-level output voltage	I_{OL} = 1 mA	0	–	0.2	V
V_{OH}	HIGH-level output voltage	I_{OH} = –1 mA	V_{CC} – 0.2	–	V_{CC}	V
Open-drain output; pin INT						
V_{OL}	LOW-level output voltage	I_{OL} = 1 mA	0	–	0.2	V
I_{OH}	HIGH-level output current	$V_{OH} = V_{CC}$	–	–	10	μA
Serial output; pins COUT, COUTQ, DOUT and DOUTQ						
$V_{o(p-p)}$	default output voltage swing (peak-to-peak value)	single-ended with 50 Ω external load; ENLOUTQ = LOW; see Figs 15 and 19; note 2	–	80	–	mV
Z_o	output impedance	single-ended to V_{CC}	80	100	120	Ω
t_r	rise time	20% to 80%	–	130	–	ps
t_f	fall time	80% to 20%	–	130	–	ps

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_{D-C}	data-to-clock delay	(COUT(Q) and DOUT(Q)) between differential cross-overs (see Fig.21)	–	170	–	ps
δ	duty cycle COUT and COUTQ	between differential cross-overs	40	50	60	%
Serial input; pins CLOOP, CLOOPQ, DLOOP, DLOOPQ						
$V_{i(p-p)}$	input voltage (peak-to-peak value)	single-ended	50	–	1000	mV
V_I	input voltage		V_{CC} – 2	–	V_{CC} + 0.25	V
Z_I	input impedance	single-ended to V_{CC}	40	50	60	Ω
t_d	delay time	see Fig.22	280	340	400	ps
t_{su}	set-up time	see Fig.22	–	30	–	ps
t_h	hold time	see Fig.22	–	30	–	ps
δ	duty cycle CLOOP and CLOOPQ	between differential cross-overs	40	50	60	%
CML mode parallel output; pins D00(Q) to D15(Q), FP(Q), PARITY(Q), POCLK(Q) and PRSCLO(Q)						
$V_{o(p-p)}$	default output voltage swing (peak-to-peak value)	single-ended with 50 Ω external load to V_{CC}; AC coupled (see Fig.19) or DC coupled (see Fig.20); note 3	–	800	–	mV
Z_o	output impedance	single-ended to V_{CC}	80	100	120	Ω
t_r	rise time	20% to 80%	–	250	–	ps
t_f	fall time	80% to 20%	–	250	–	ps
f_P	parallel bit rate		–	–	400	Mbits/s
LVPECL mode parallel output; pins D00(Q) to D15(Q), FP(Q), PARITY(Q), POCLK(Q) and PRSCLO(Q)						
V_{OH}	HIGH-level output voltage	50 Ω termination to V_{CC} – 2V (see Fig.16)	V_{CC} – 1.2	–	V_{CC} – 0.9	V
V_{OL}	LOW-level output voltage	50 Ω termination to V_{CC} – 2V (see Fig.16)	V_{CC} – 2.2	–	V_{CC} – 1.7	V
$V_{o(p-p)}$	default output voltage swing (peak-to-peak value)	LVPECL floating (see Fig.13); single-ended with 50 Ω external load to V_{CC}; AC coupled (see Fig.18) or DC coupled (see Fig.17); note 3	–	800	–	mV
t_r	rise time	20% to 80%	–	350	–	ps
t_f	fall time	80% to 20%	–	350	–	ps
f_P	parallel bit rate		–	–	400	Mbits/s

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Timing parallel output; pins D00(Q) to D15(Q), FP(Q), PARITY(Q), POCLK(Q) and PRSCLO(Q) (see Fig.23)						
t_{D-C}	data-to-clock delay D00 to D15/POCLK	DMX 1 : 16, 1 : 10, 1 : 8; see Fig.23; note 4	100	100	250	ps
t_{D-C}	data-to-clock delay D06 to D09/POCLK	DMX 1 : 4; see Fig.23; note 4	150	180	300	ps
δ	duty cycle POCLK		40	50	60	%
skew	channel to channel skew D00 and Dn (between channels)	DMX 1 : 16, 1 : 10, 1 : 8; note 4	–	–	200	ps
skew	channel to channel skew D06 and D09 (between channels)	DMX 1 : 4; note 4	–	–	50	ps
Reference; pin RREF						
V_{ref}	reference voltage	10 to 20 kΩ resistor to V_{EE}	1.17	1.22	1.28	V
I²C-bus pins SCL and SDA						
V_{IL}	LOW-level input voltage		0	–	$0.3V_{CC}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{CC}$	–	V_{CC}	V
V_{hys}	hysteresis of Schmitt trigger inputs		$0.05V_{CC}$	–	–	V
V_{OL}	SDA LOW-level output voltage (open-drain)	I_{OL} = 3 mA	0	–	0.4	V
I_L	leakage current		–10	–	+10	µA
C_i	input capacitance		–	–	10	pF
I²C-bus timing						
f_{SCL}	SCL clock frequency		–	–	100	kHz
t_{LOW}	SCL LOW time		1.3	–	–	µs
$t_{HD;STA}$	hold time START condition		0.6	–	–	µs
t_{HIGH}	SCL HIGH time		0.6	–	–	µs
$t_{SU;STA}$	set-up time START condition		0.6	–	–	µs
$t_{HD;DAT}$	data hold time		0	–	0.9	µs
$t_{SU;DAT}$	data set-up time		100	–	–	ns
$t_{SU;STO}$	set-up time STOP condition		0.6	–	–	µs
t_r	SCL and SDA rise time		20	–	300	ns
t_f	SCL and SDA fall time		20	–	300	ns
t_{BUF}	bus free time between STOP and START		1.3	–	–	µs
C_b	capacitive load for each bus line		–	–	400	pF
t_{SP}	pulse width of allowable spikes		0	–	50	ns
V_{nL}	noise margin at LOW level		$0.1V_{CC}$	–	–	V
V_{nH}	noise margin at HIGH level		$0.2V_{CC}$	–	–	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
RF input; pins IN1, INQ1, IN2 and IN2Q						
$V_{i(p-p)}$	input voltage swing (peak-to-peak value)	single-ended; note 7	12	–	500	mV
V_{sl}	typical slice level range	note 5	–50	–	+50	
Z_i	input impedance	differential	80	100	120	Ω
α_{iso}	between channel isolation		–	60	–	dB
Received Signal Strength Indicator (RSSI)						
$V_{i(p-p)}$	input voltage swing (peak-to-peak value)	single-ended	5	–	500	mV
S_{RSSI}	RSSI sensitivity	see Fig.3	15	17	19	mV/dB
$V_{RSSI(30mV)}$	output voltage	V_i = 30 mV (p-p); PRBS (2^{31}-1)	560	650	740	mV
ΔV_{RSSI}	output voltage variation	input 30 to 3200 Mbits/s; PRBS (2^{31}-1); V_{CC} = 3.14 to 3.47 V; ΔT = 120 °C	–50	–	+50	mV
Output; pins RSSI1 and RSSI2						
Z_o	output impedance		–	1	10	Ω
$I_{O(source)}$	output source current		–	–	1	mA
$I_{O(sink)}$	output sink current		–	–	0.4	mA
LOS detector						
hys	hysteresis	note 6	–	2.5	–	dB
t_a	assert time	$\Delta V_{i(p-p)}$ = 3 dB	–	–	5	µs
t_d	de-assert time	$\Delta V_{i(p-p)}$ = 3 dB	–	–	5	µs
Reference frequency input; pins CREF and CREFQ						
$V_{i(p-p)}$	input voltage (peak-to-peak value)	single-ended	50	–	1000	mV
V_I	input voltage		V_{CC} – 1	–	V_{CC} + 0.25	V
Z_i	input impedance	single-ended to V_{CC}	40	50	60	Ω
Δf_{CREF}	reference clock frequency accuracy requirement	for SDH/SONET operation	–20	–	+20	ppm
f_{CREF}	reference clock frequency	see Table 8; R = 1, 2, 4 or 8	18 × R	19.44 × R	21 × R	MHz
PLL characteristics						
t_{acq}	acquisition time	30 Mbits/s	–	–	200	µs
$t_{acq(pc)}$	acquisition time at power cycle	30 Mbits/s	–	–	10	ms
$t_{acq(o)}$	acquisition time octave change	30 Mbits/s	–	–	10	µs
TDR	transitionless data run	30 Mbits/s	–	1000	–	bits

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Jitter tolerance						
$J_{tol(p-p)}$	jitter tolerance (peak-to-peak value)	STM1/OC3 mode (ITU-T G.958); PRBS (2^{31}-1)				
		f = 6.5 kHz	3	>10	–	UI
		f = 65 kHz	0.3	>1	–	UI
		f = 1 MHz	0.3	>0.5	–	UI
		STM4/OC12 mode (ITU-T G.958); PRBS (2^{31}-1)				
		f = 25 kHz	3	>10	–	UI
		f = 250 kHz	0.3	>1	–	UI
		f = 5 MHz	0.3	>0.5	–	UI
		STM16/OC48 mode (ITU-T G.958); PRBS (2^{31}-1)				
		f = 100 kHz	3	10	–	UI
		f = 1 MHz	0.3	1	–	UI
		f = 20 MHz	0.3	0.5	–	UI

Notes

1. Default settings: UI = LOW (pre-programmed mode, see Table 1); DR0 = LOW, DR1 = HIGH, DR2 = LOW (STM16/OC48); INSEL = HIGH (limiter 1 is active); WINSIZE = HIGH (1000 ppm); ENBA = HIGH (automatic byte alignment); ENLOUTQ = HIGH (DOUT, COUT disabled); ENLINQ = HIGH (DLOOP, CLOOP disabled); DMXR0 = HIGH, DMXR1 = HIGH (DMX ratio is 1 : 16); CREF(Q) = 19.44 MHz; LOSTH2 is not connected (LOS2 switched off); D00(Q) to D15(Q), FP(Q), PARITY(Q), POCLK(Q) and PRSCLO(Q) are not connected.
2. The output swing is adjustable in 16 steps controlled by bits RFS in I^2C-bus register CBH.
3. The output swing is adjustable in 16 steps controlled by bits MFS in I^2C-bus register C8H. In standard LVPECL mode only swing = 12 (default) should be used.
4. With 50% duty cycle.
5. The slice level is adjustable in 256 steps controlled by I^2C-bus registers C0H and C1H.
6. The hysteresis is adjustable in 8 steps controlled by bits HYS1 and HYS2 in I^2C-bus registers BDH and BFH.
7. The RF input is protected against a differential overvoltage; the maximum input current is 30 mA.

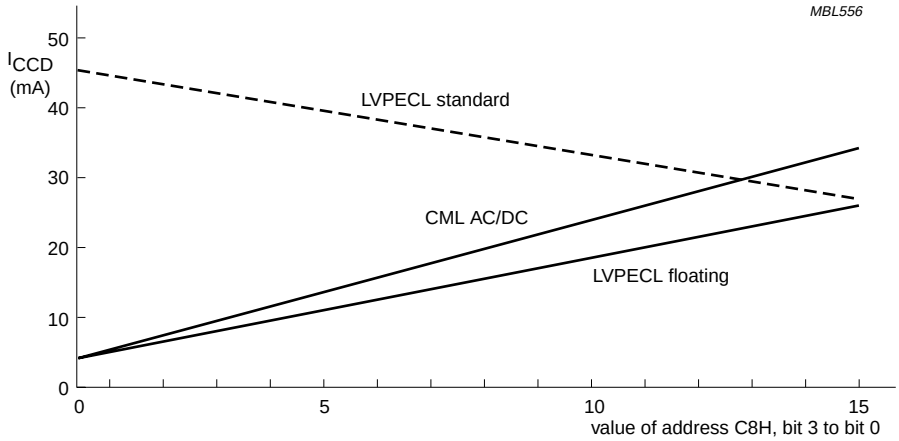


Fig.12 Suply current per parallel output.

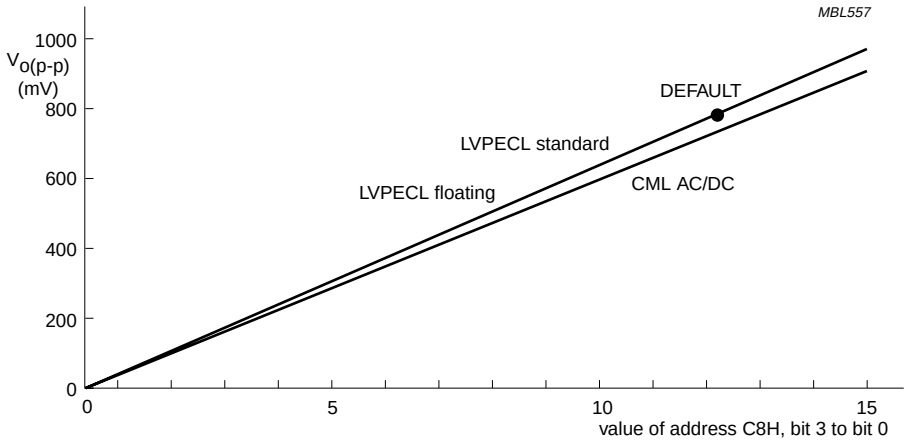
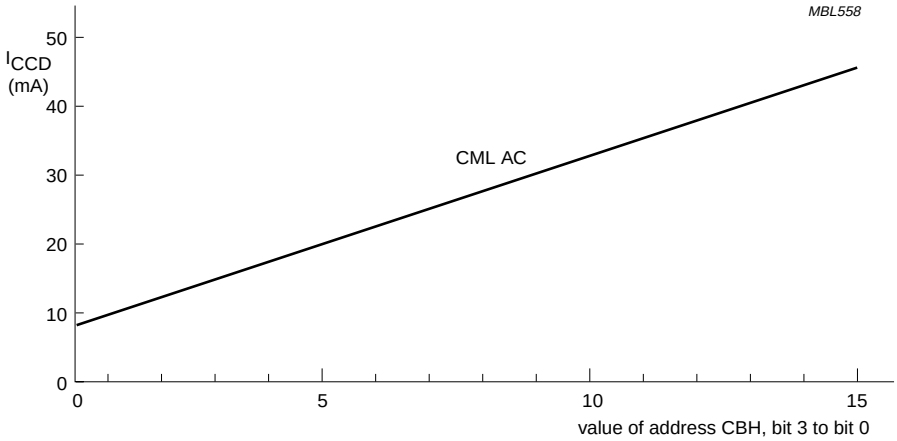


Fig.13 Output voltage swing of parallel output.



Serial outputs are default off.

Fig.14 Supply current per serial output.

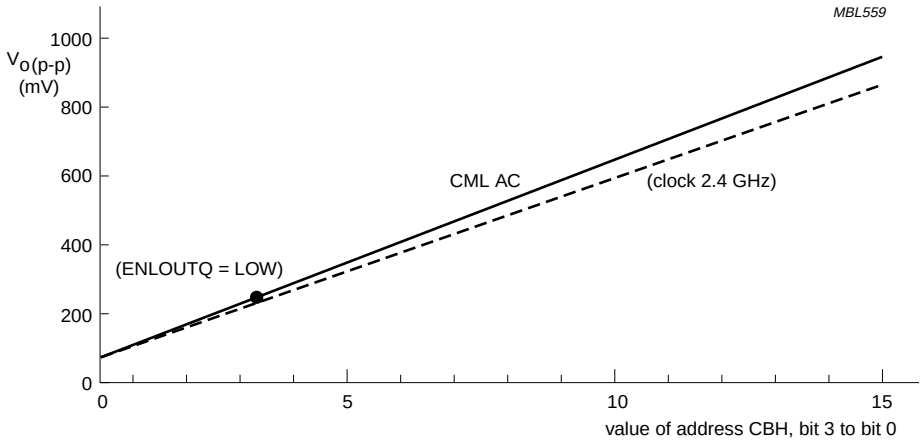


Fig.15 Output voltage swing of serial output.

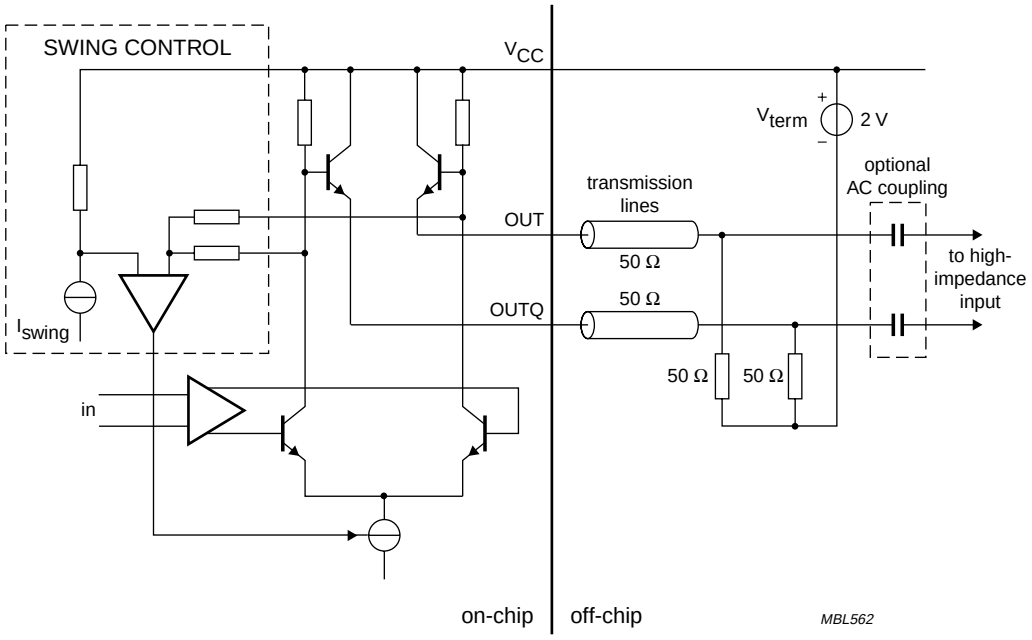


Fig.16 Standard PECL mode.

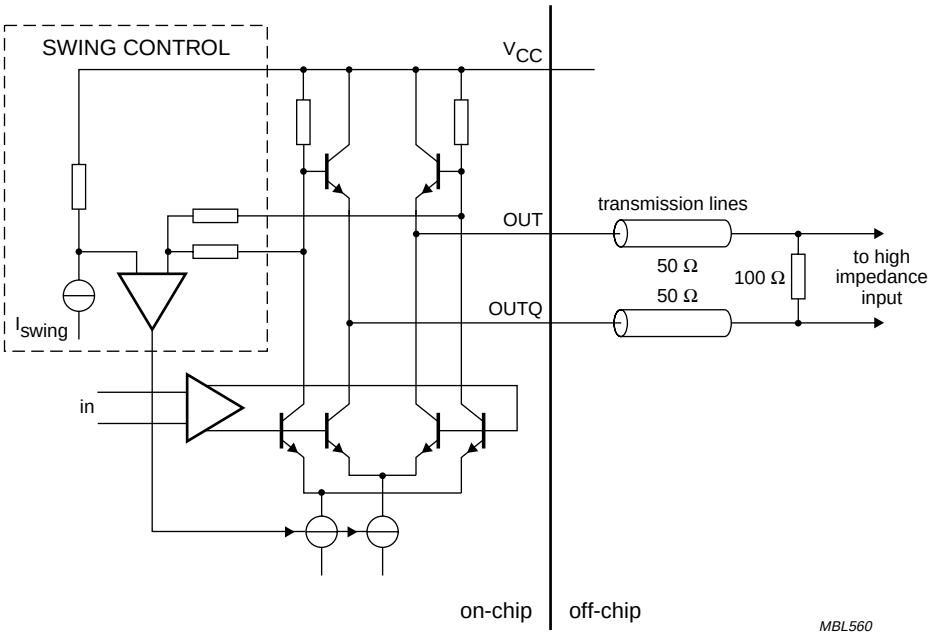


Fig.17 Floating PECL mode (DC coupled).

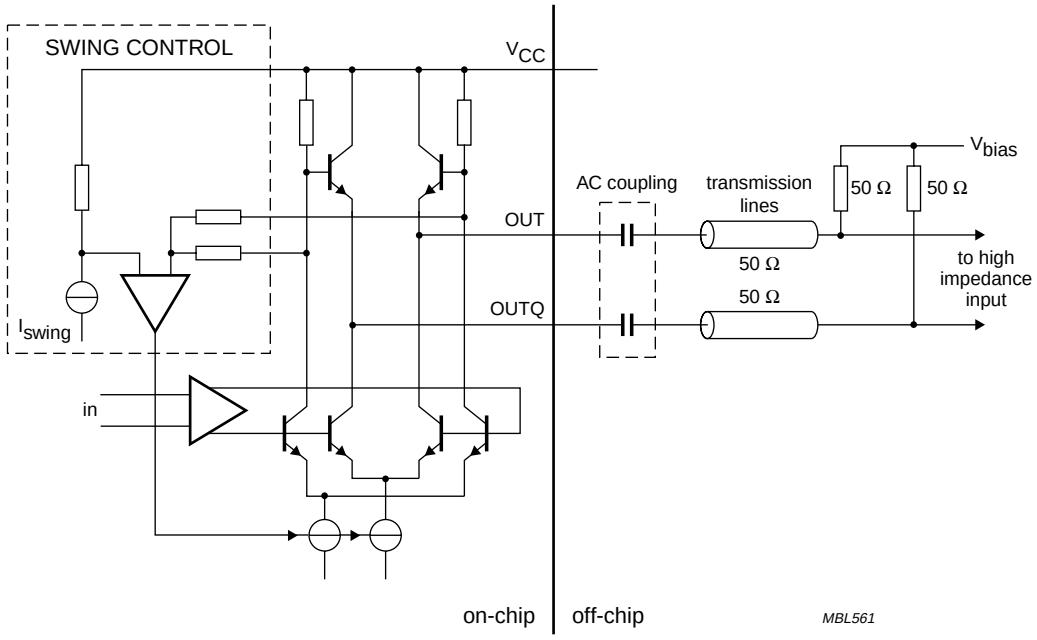


Fig.18 Floating LVPECL mode (AC coupled).

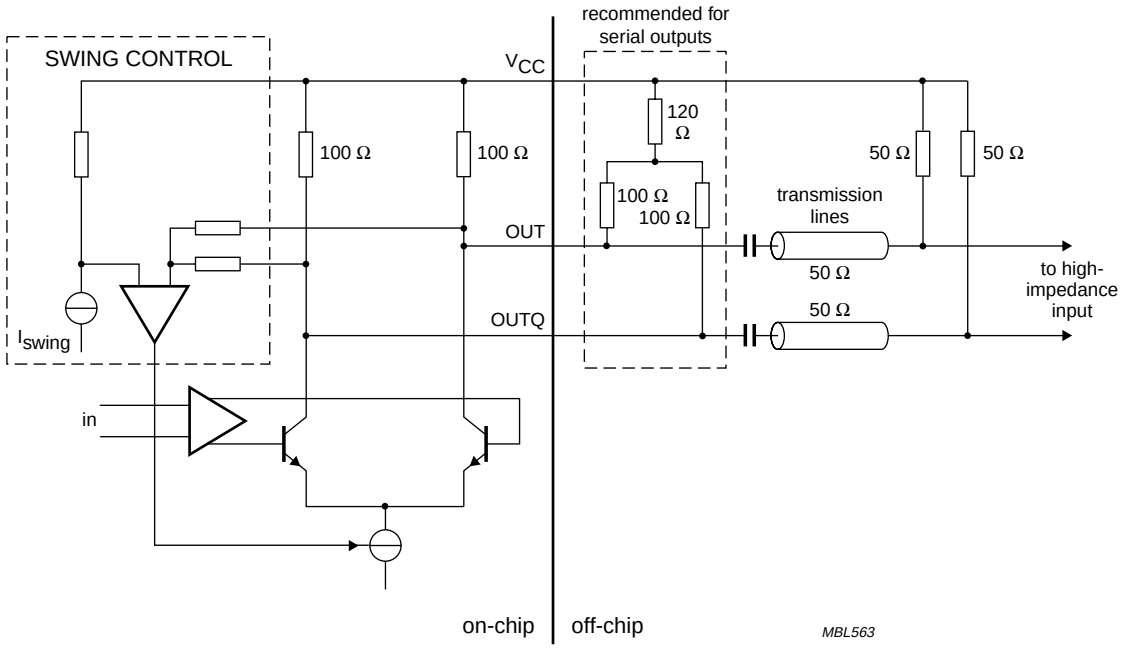


Fig.19 CML AC coupled mode.

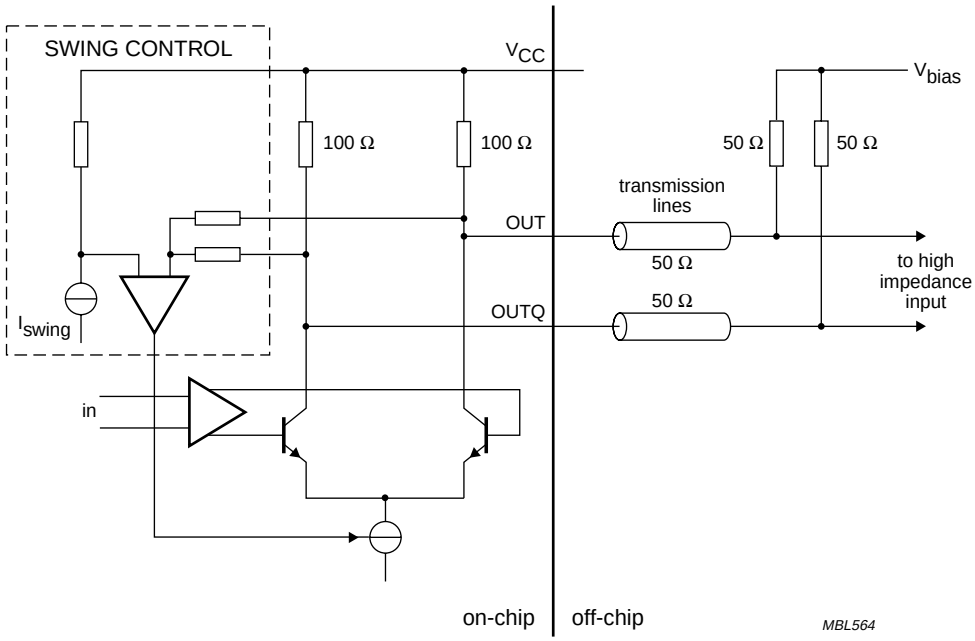
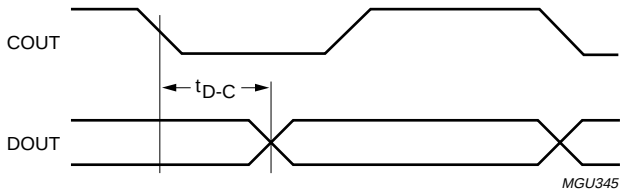
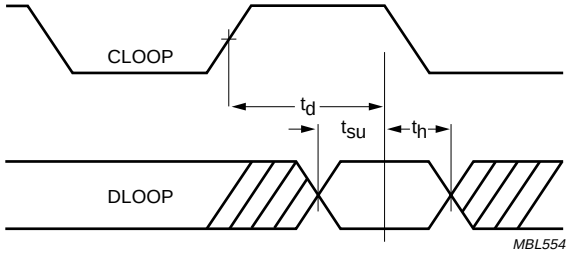


Fig.20 CML DC coupled mode.



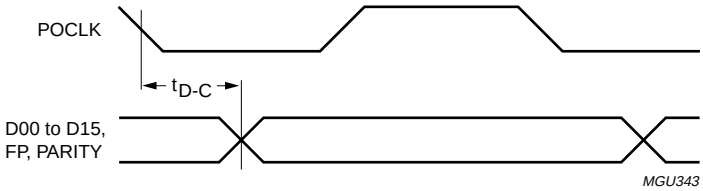
The timing is measured from the cross-over point of the clock output signal to the cross-over point of the data output (all signals are differential).

Fig.21 Loop mode output timing.



The timing is measured from the cross-over point of the clock input signal to the cross-over point of the data input.

Fig.22 Loop mode input timing.

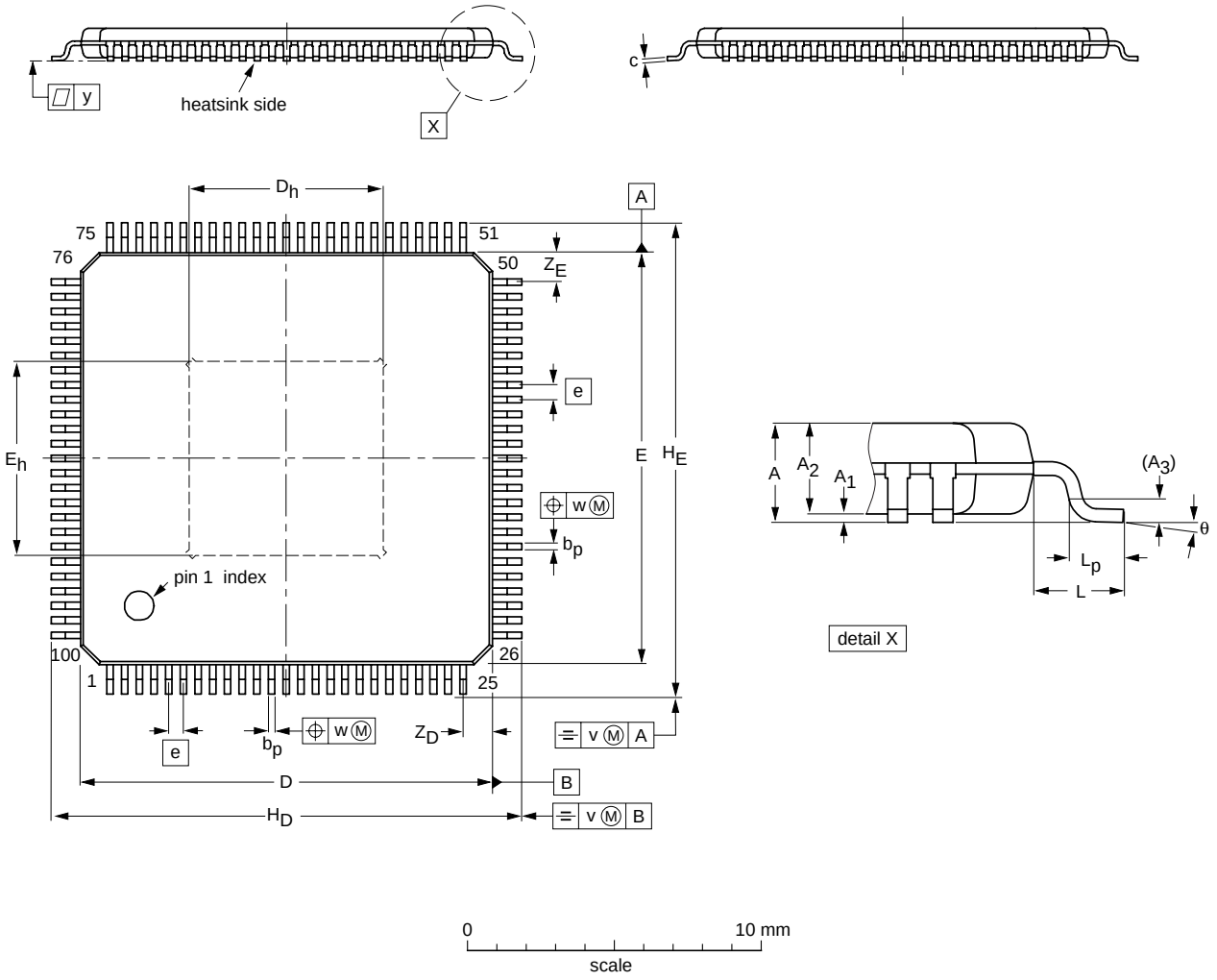


The timing is measured from the cross-over point of the clock output signal to the cross-over point of the data output (all signals are differential).

Fig.23 Parallel bus output timing.

PACKAGE OUTLINE

HTQFP100: plastic, heatsink thin quad flat package; 100 leads; body 14 x 14 x 1.0 mm **SOT638-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.2	0.15 0.05	1.05 0.95	0.25	0.27 0.17	0.20 0.09	14.1 13.9	7.1 6.1	14.1 13.9	7.1 6.1	0.5	16.15 15.85	16.15 15.85	1.0	0.75 0.45	0.2	0.08	0.08	1.15 0.85	1.15 0.85	7° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT638-1						01-03-30

SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 220 °C for thick/large packages, and below 235 °C for small/thin packages.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE[1]	SOLDERING METHOD	
	WAVE	REFLOW[2]
BGA, LBGA, LFBGA, SQFP, TFBGA, VFBGA	not suitable	suitable
HBCC, HBGA, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable[3]	suitable
PLCC[4], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended[4][5]	suitable
SSOP, TSSOP, VSO	not recommended[6]	suitable

Notes

1. For more detailed information on the BGA packages refer to the *"(LF)BGA Application Note*" (AN01026); order a copy from your Philips Semiconductors sales office.
2. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
3. These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.
4. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
5. Wave soldering is suitable for LQFP, TQFP and QFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
6. Wave soldering is suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

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DATA SHEET STATUS(1)	PRODUCT STATUS(2)	DEFINITIONS
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NOTES

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